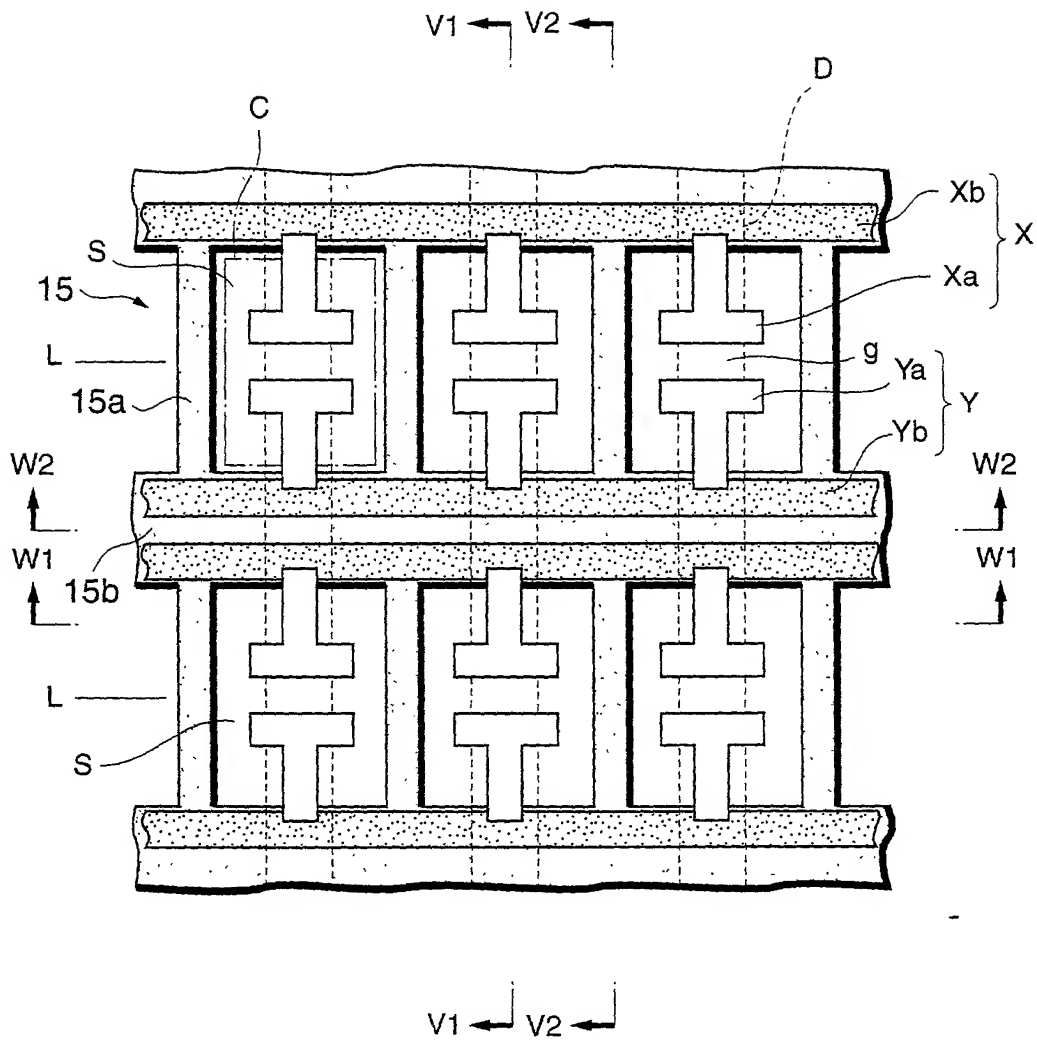
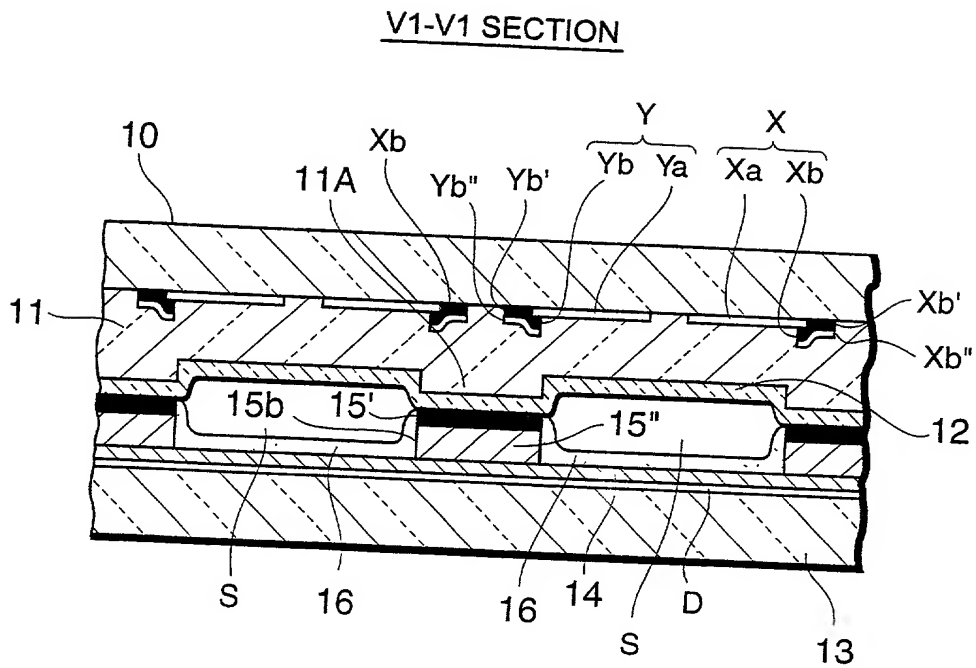
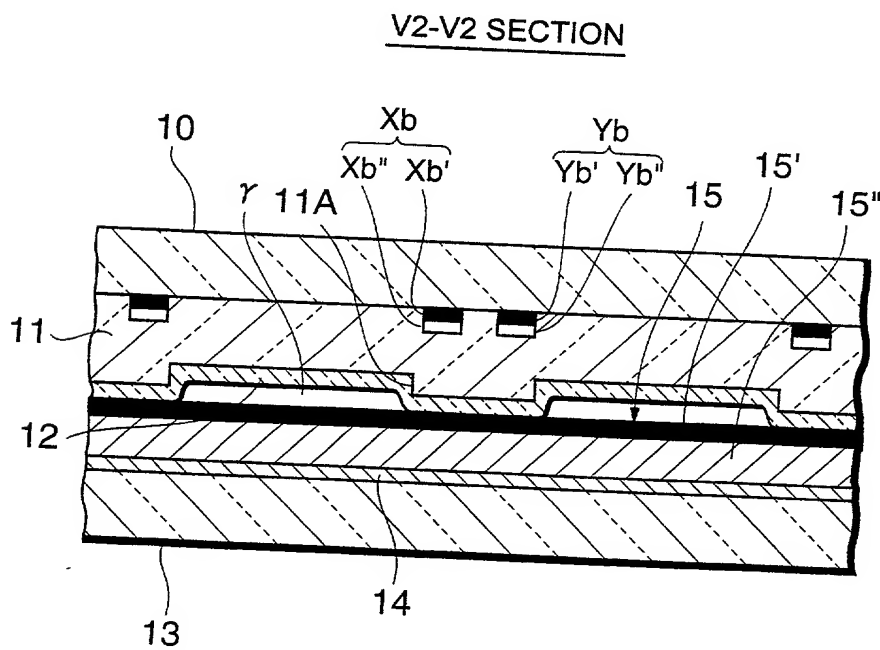
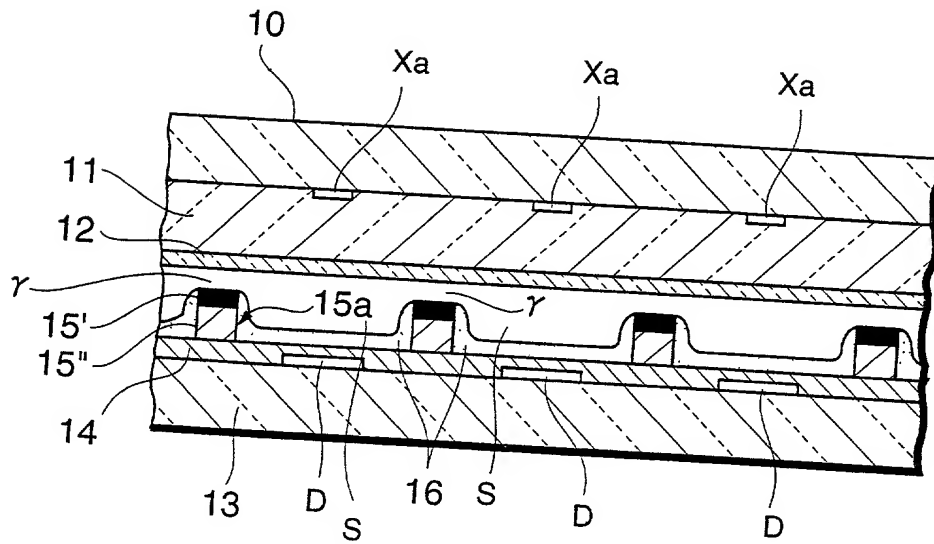
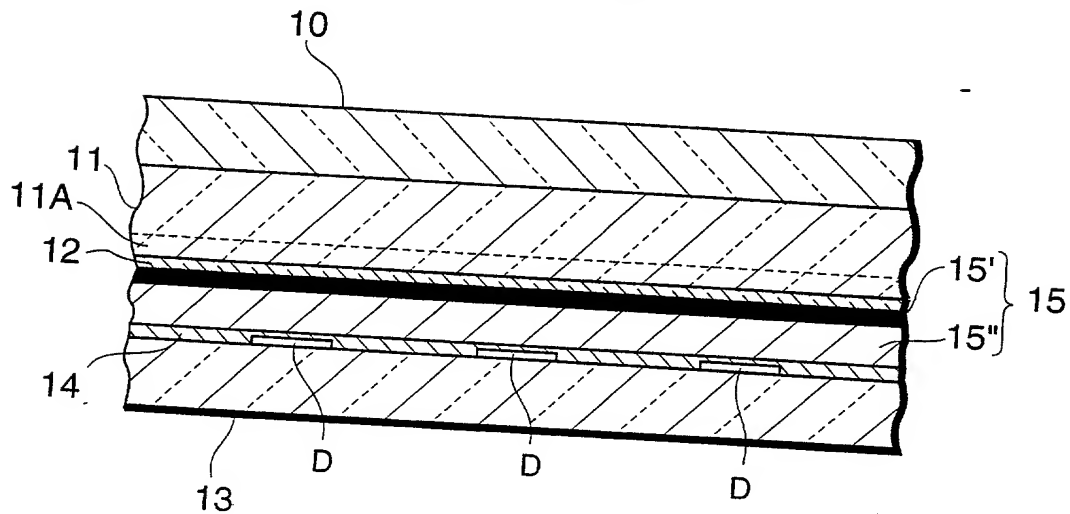
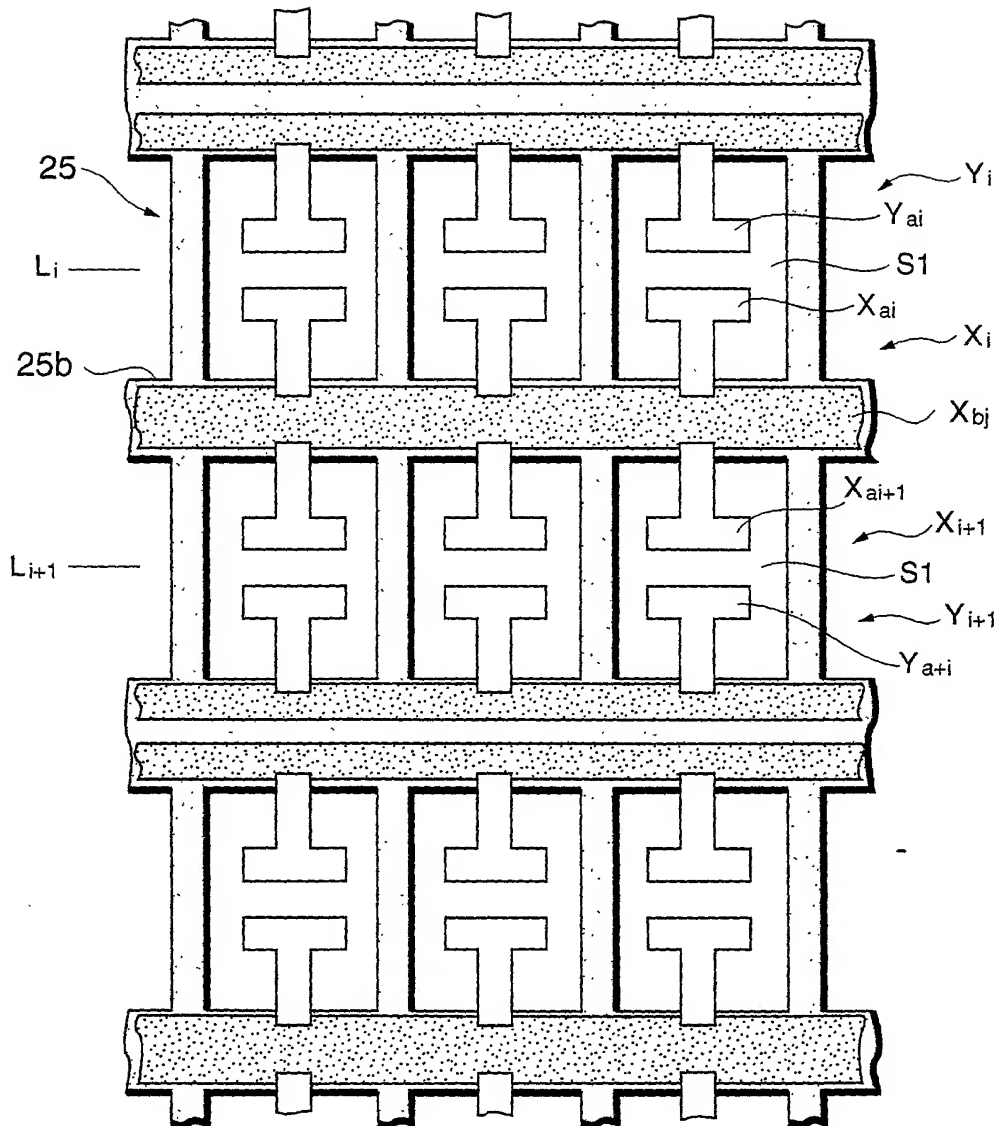
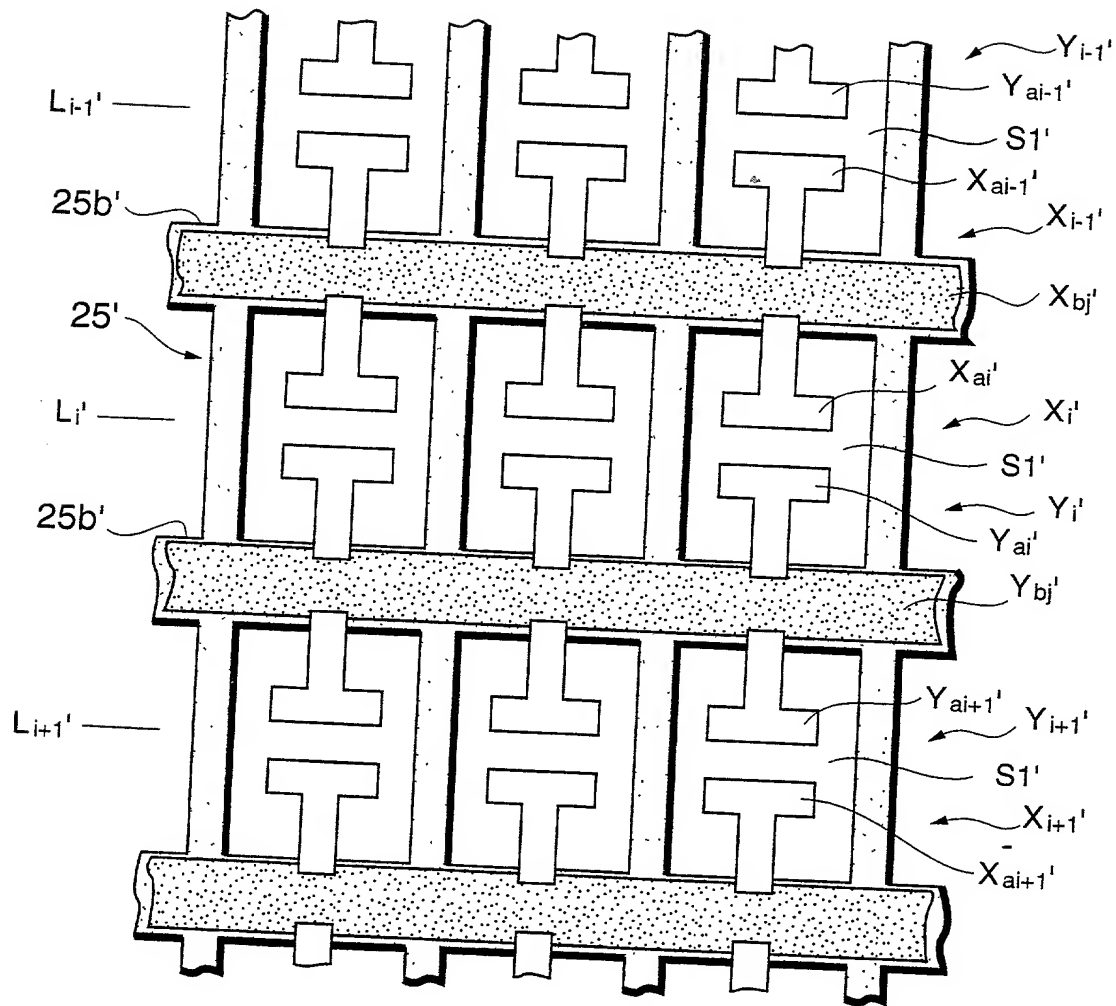


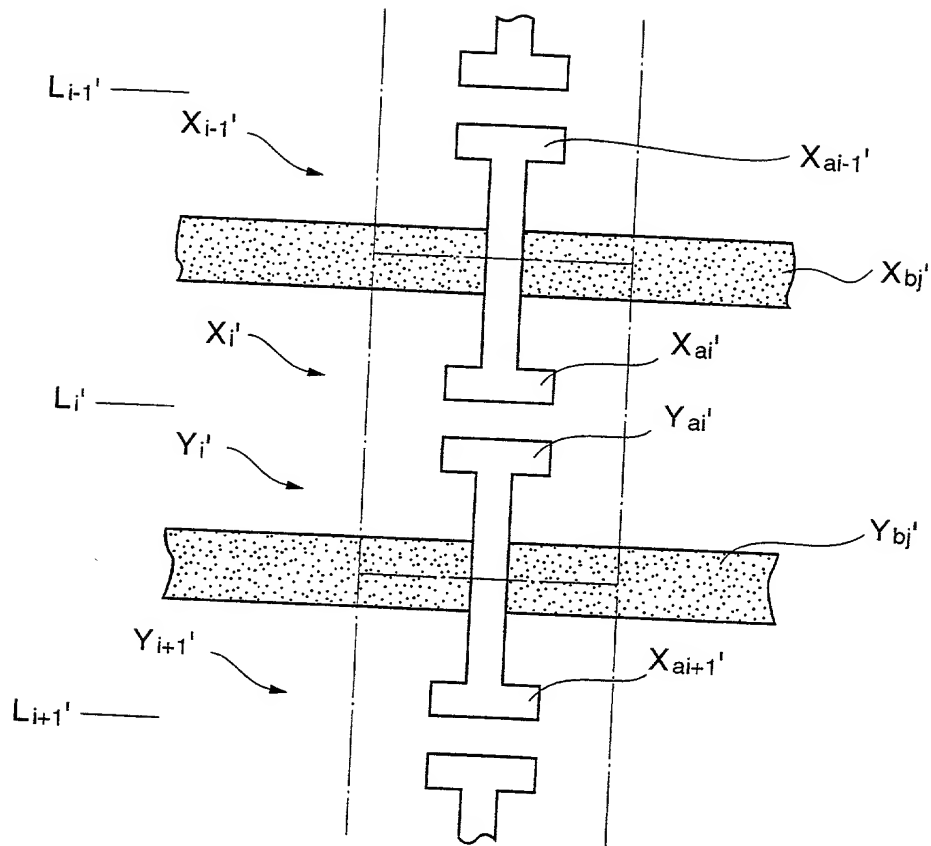
**Fig. 1**

**Fig.2****Fig.3**

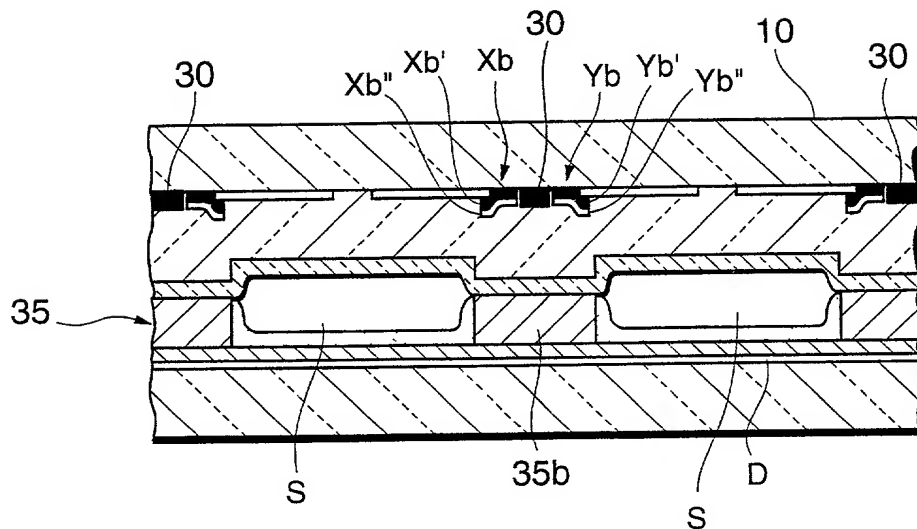
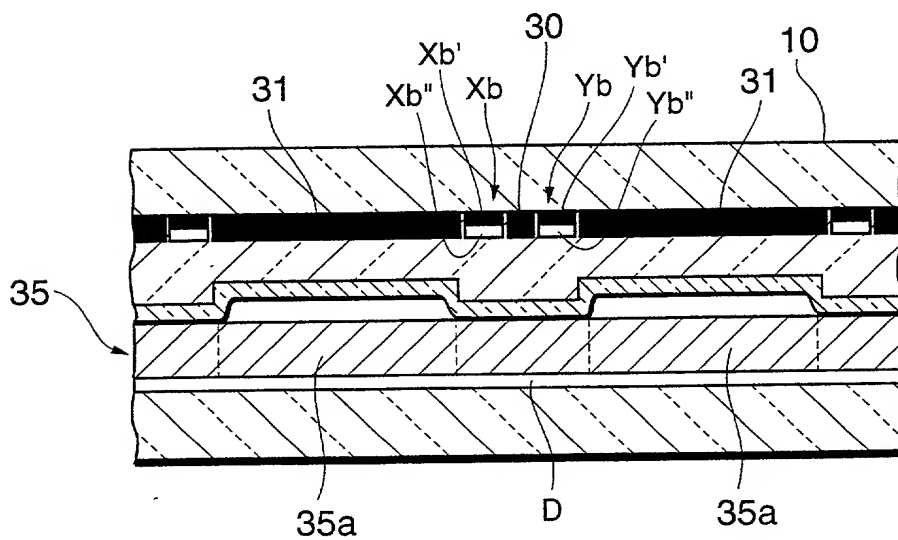
**Fig.4**W1-W1 SECTION**Fig.5**W2-W2 SECTION

**Fig.6**

**Fig.7**

**Fig.8**

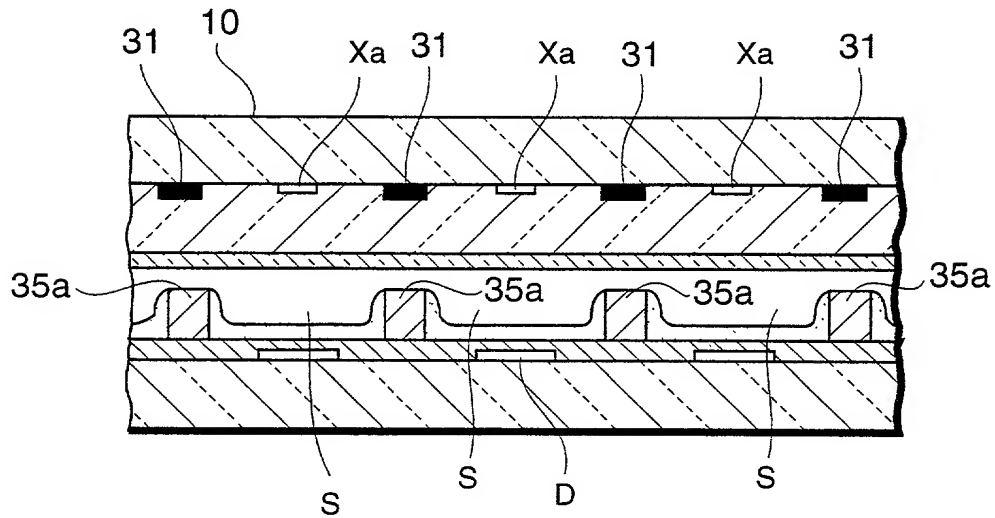
The diagram shows a cross-section of a semiconductor device with two identical stacked layers. Each layer consists of a substrate with a grid of conductive patterns (labeled 30) interconnected by vertical vias (labeled 31). The top layer has an additional passivation layer (labeled S) and a contact layer (labeled L) on its upper surface. Dimensional parameters are defined as follows: W3 is the width of the conductive patterns; W4 is the width of the vias; V3 is the pitch between the centers of adjacent patterns; and V4 is the pitch between the centers of adjacent vias. Coordinate systems (X, Y) are shown for both layers.

**Fig. 10**V3-V3 SECTION**Fig. 11**V4-V4 SECTION



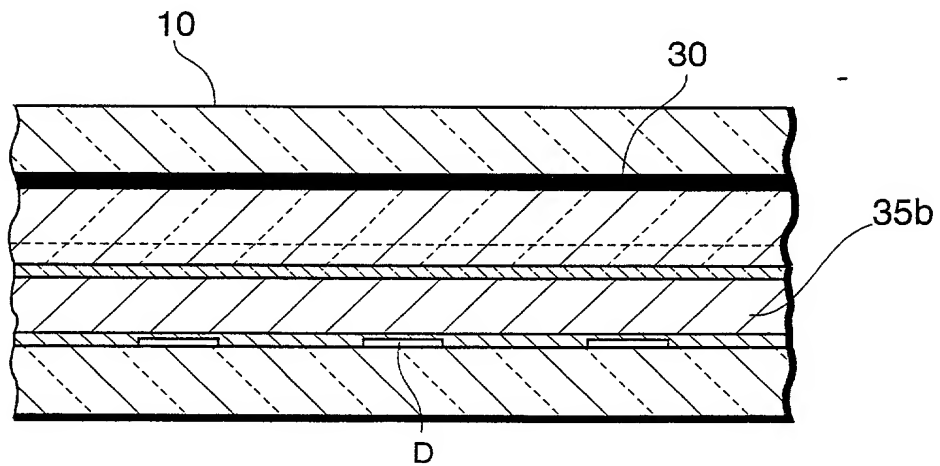
**Fig.12**

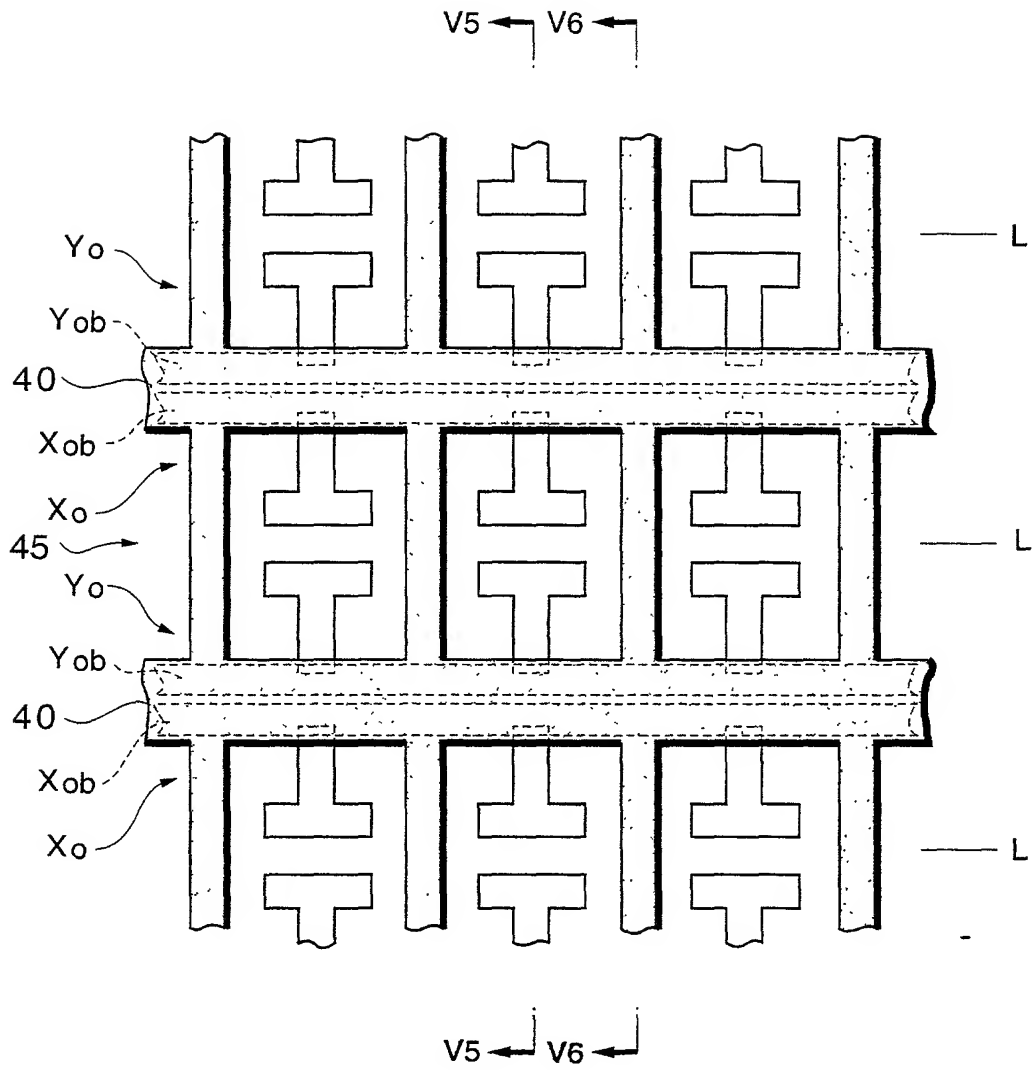
W3-W3 SECTION



**Fig.13**

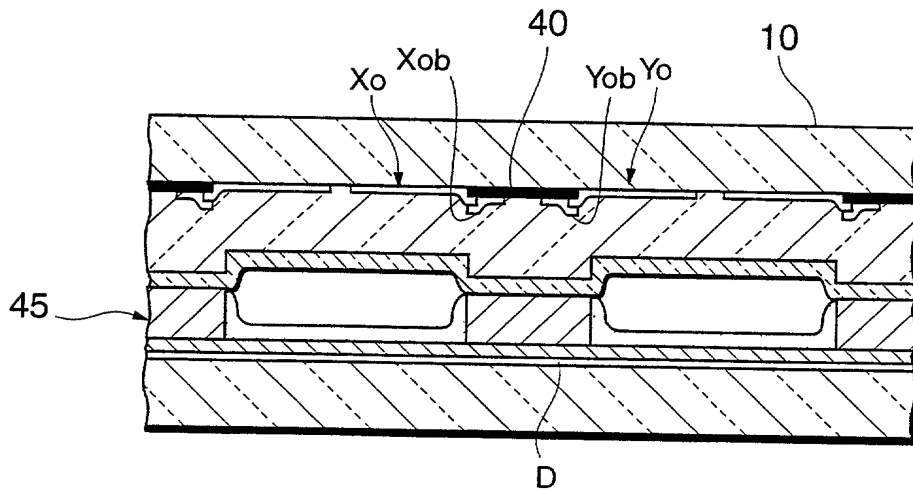
W4-W4 SECTION



**Fig.14**

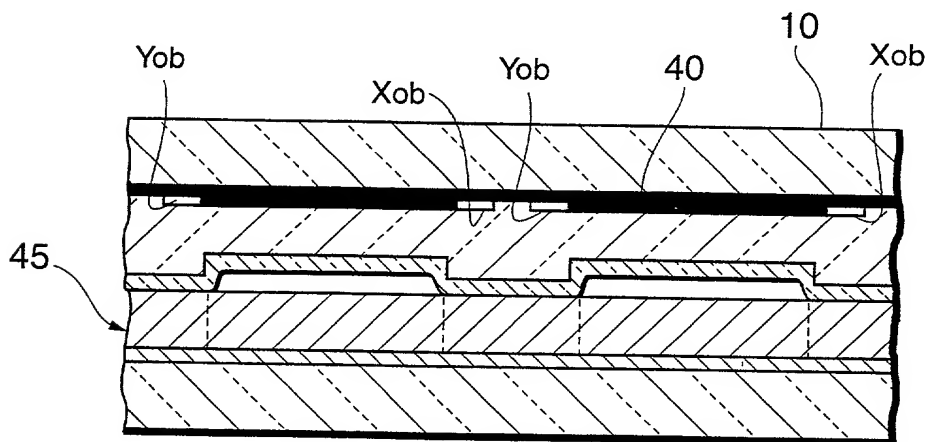
**Fig. 15**

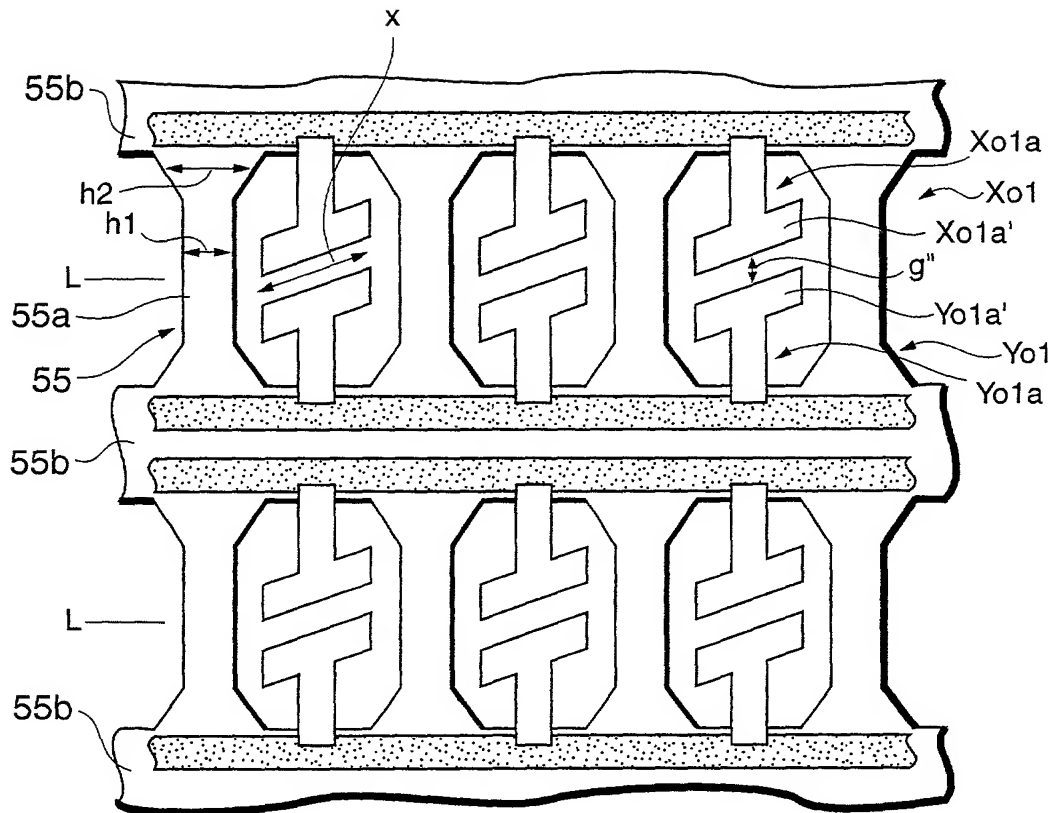
V5-V5 SECTION

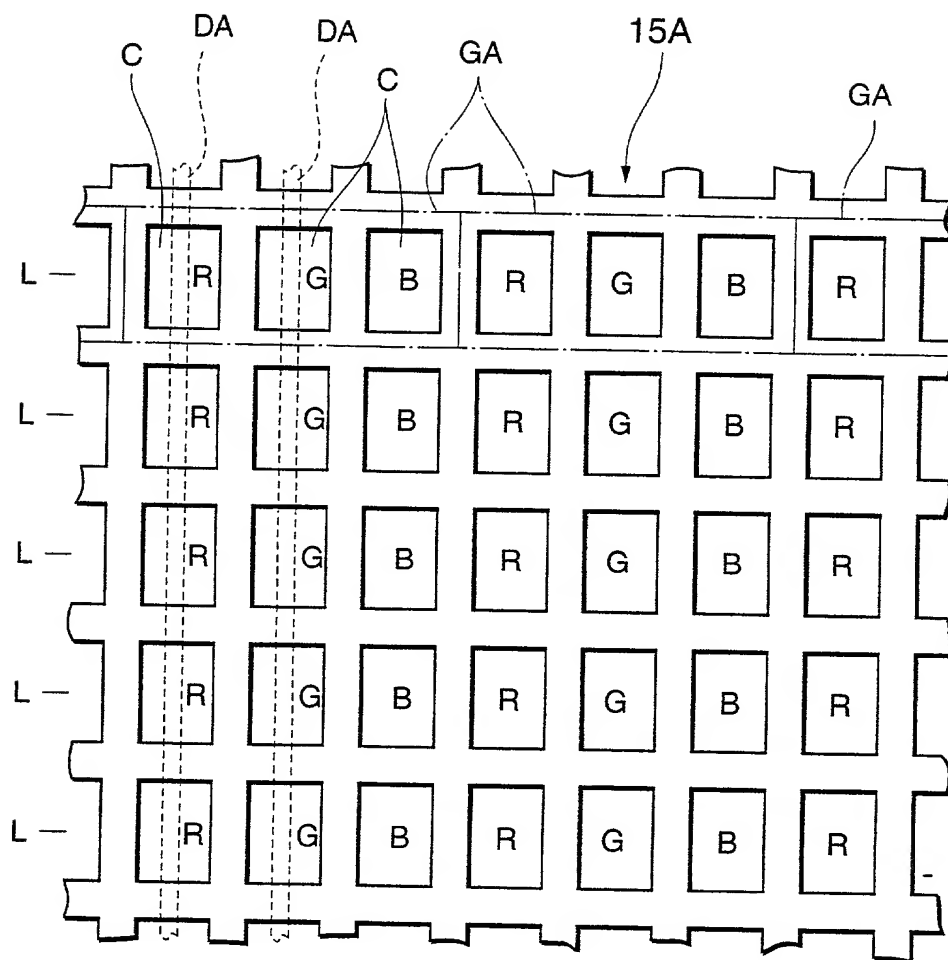


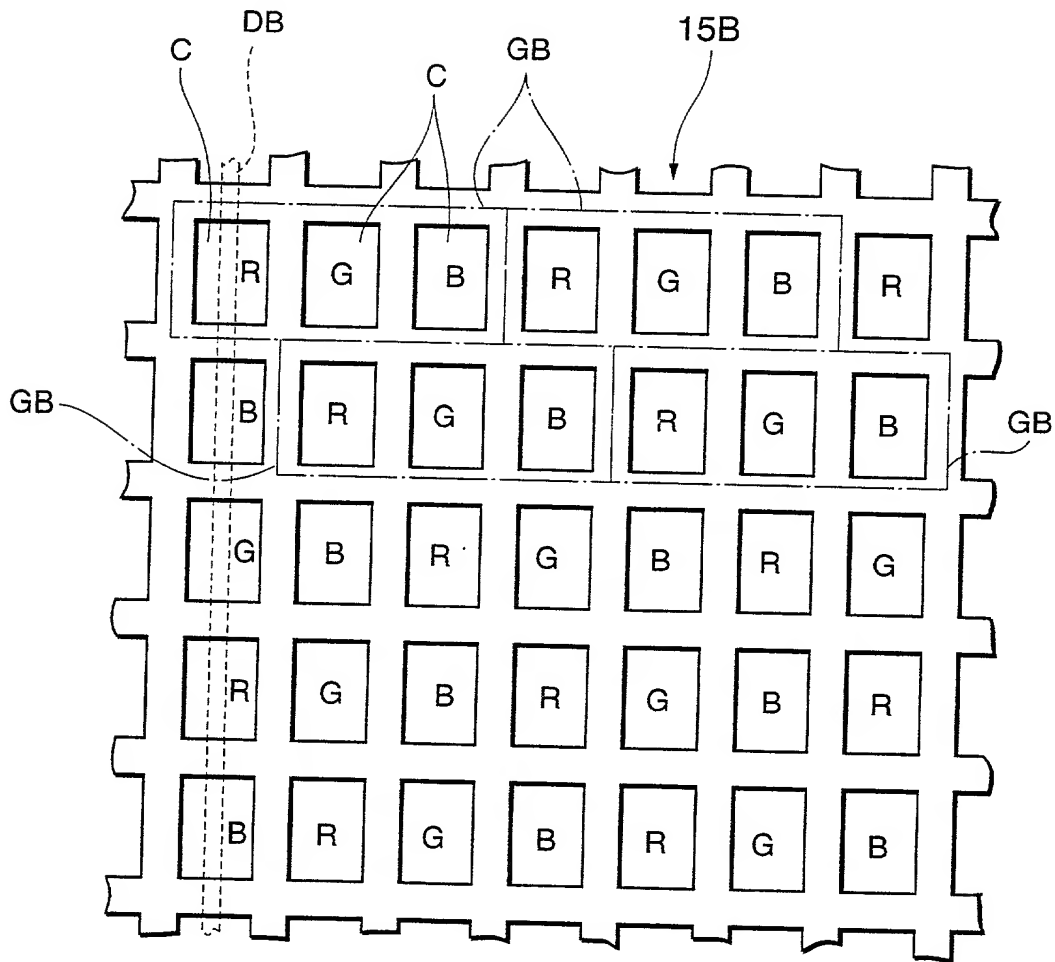
**Fig. 16**

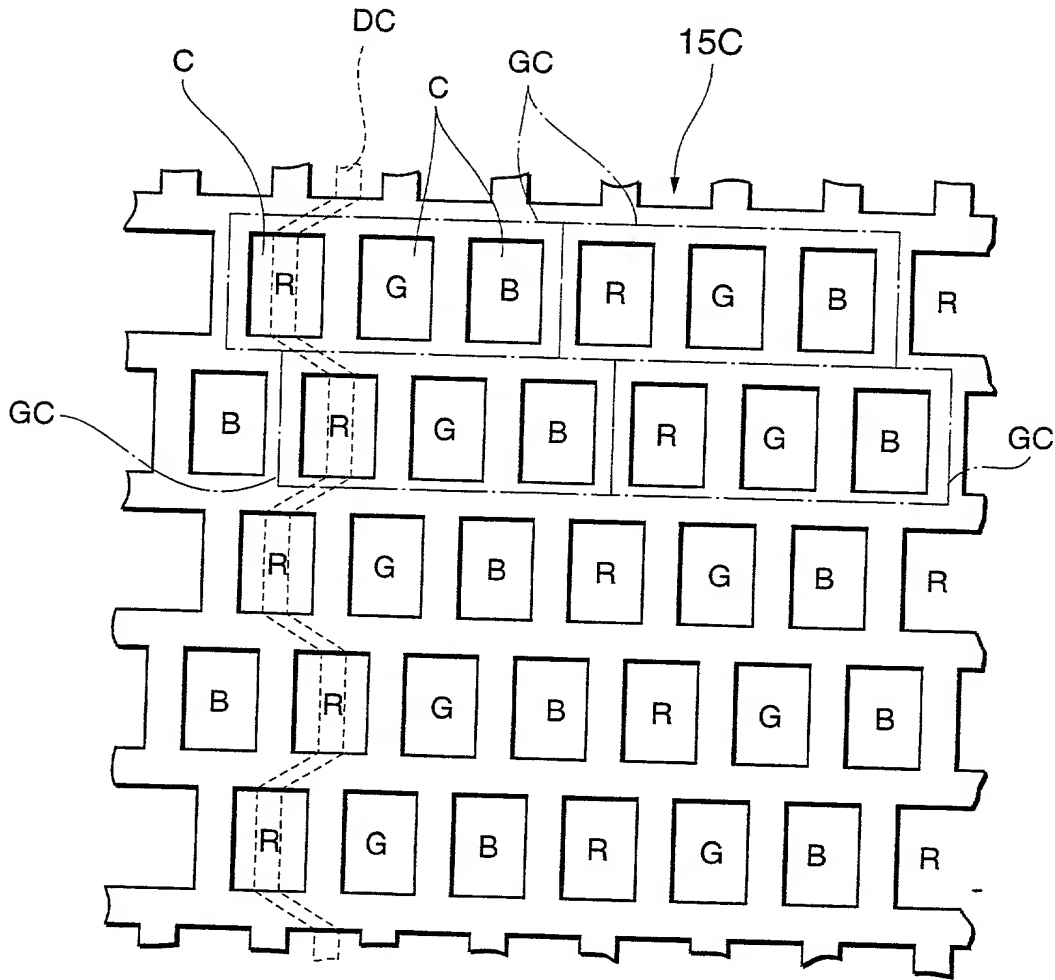
V6-V6 SECTION

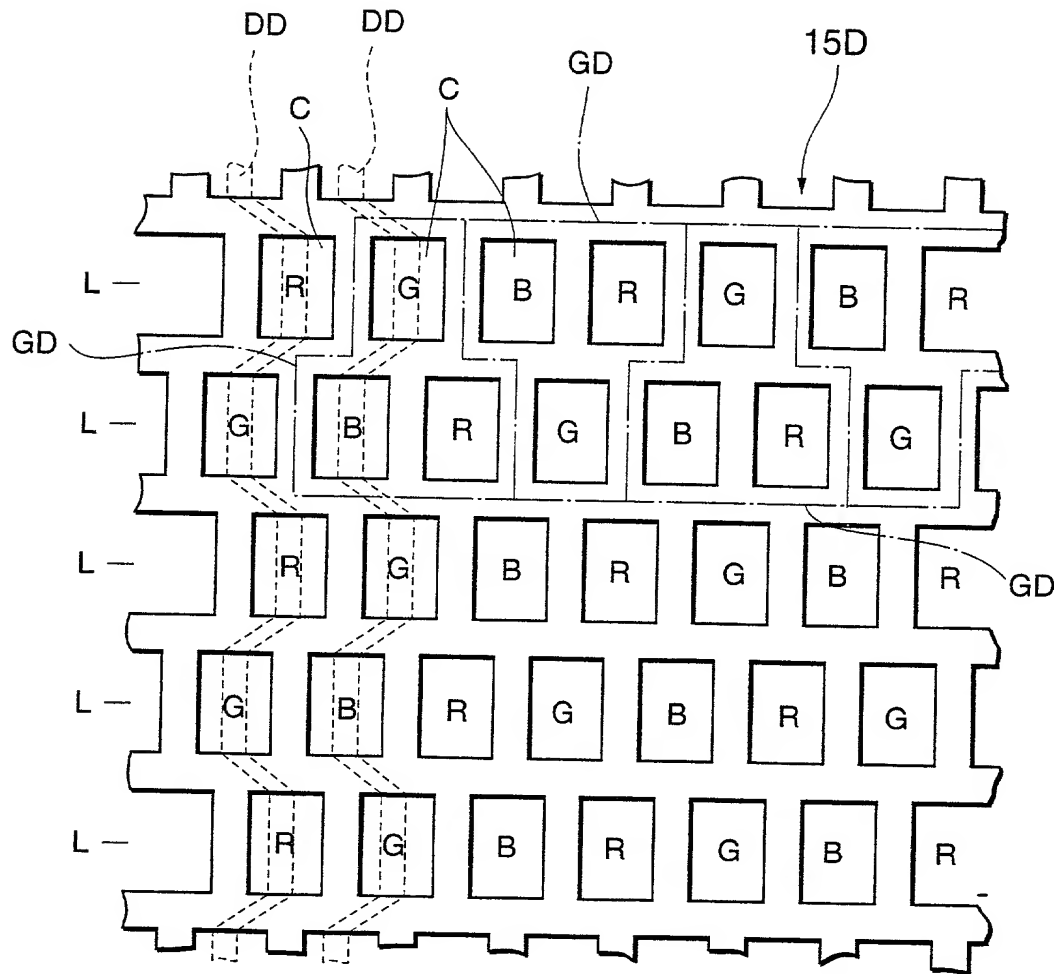


**Fig.17**

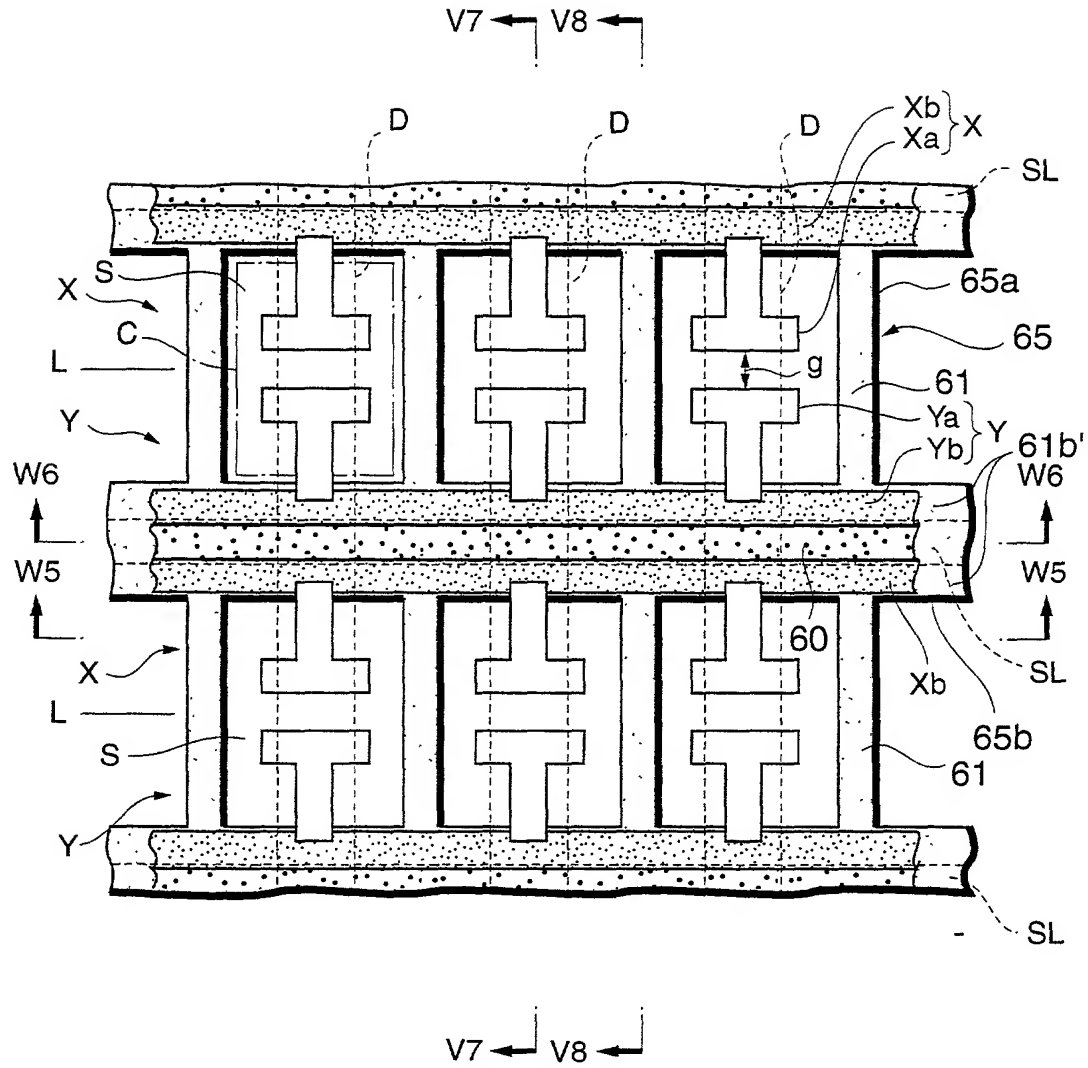
**Fig. 18**

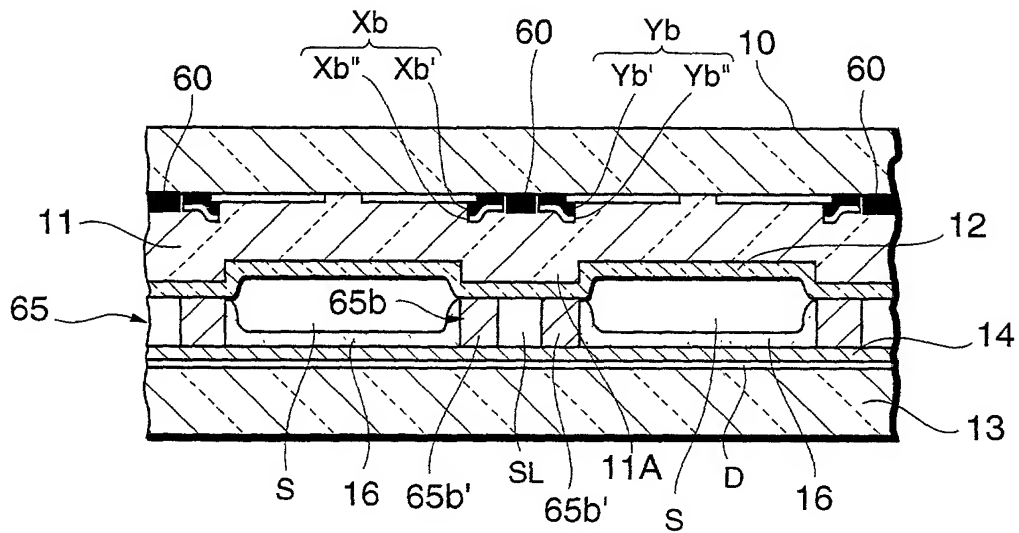
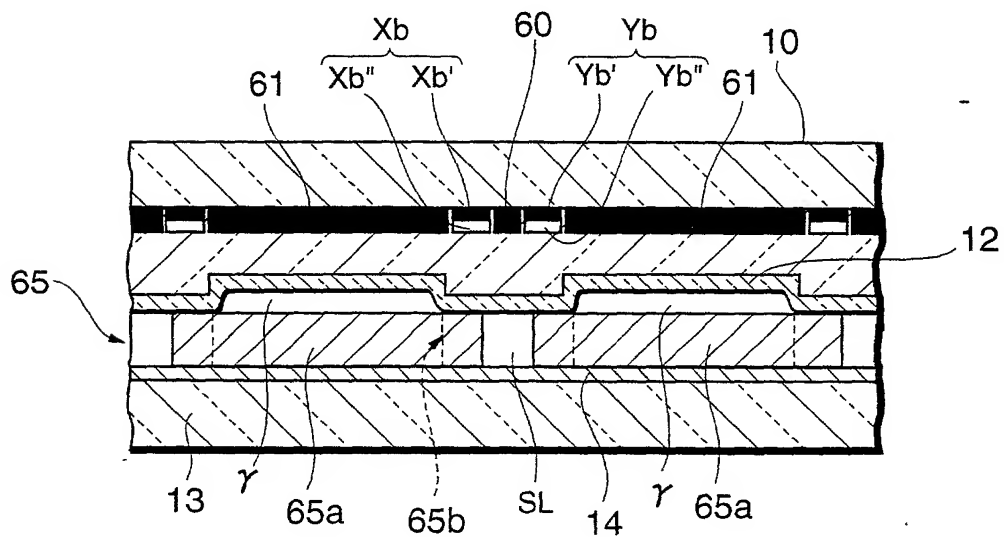
**Fig. 19**

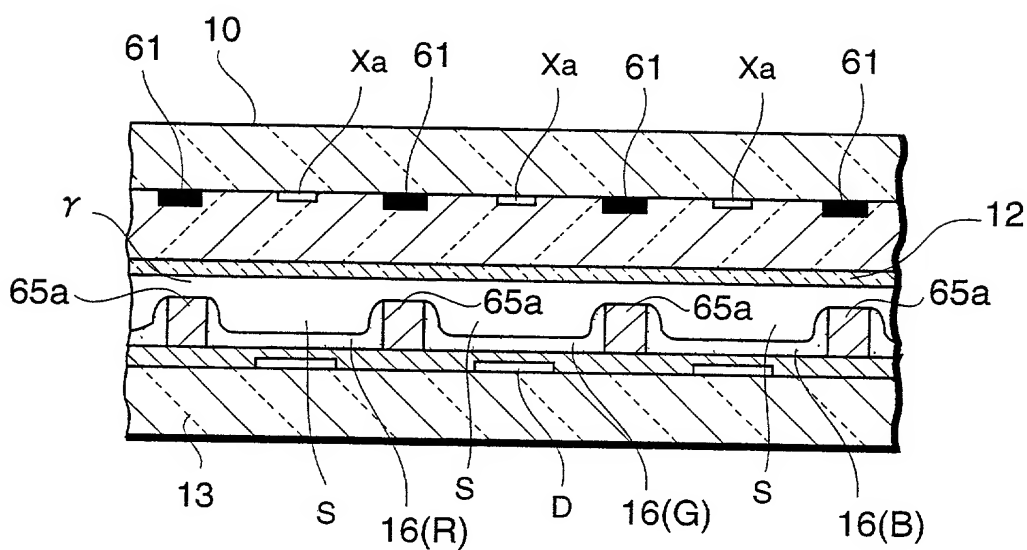
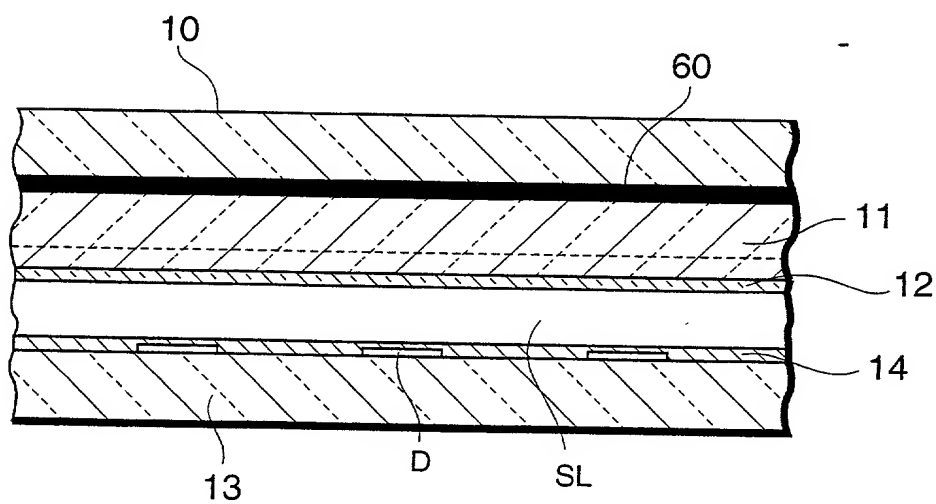
**Fig.20**

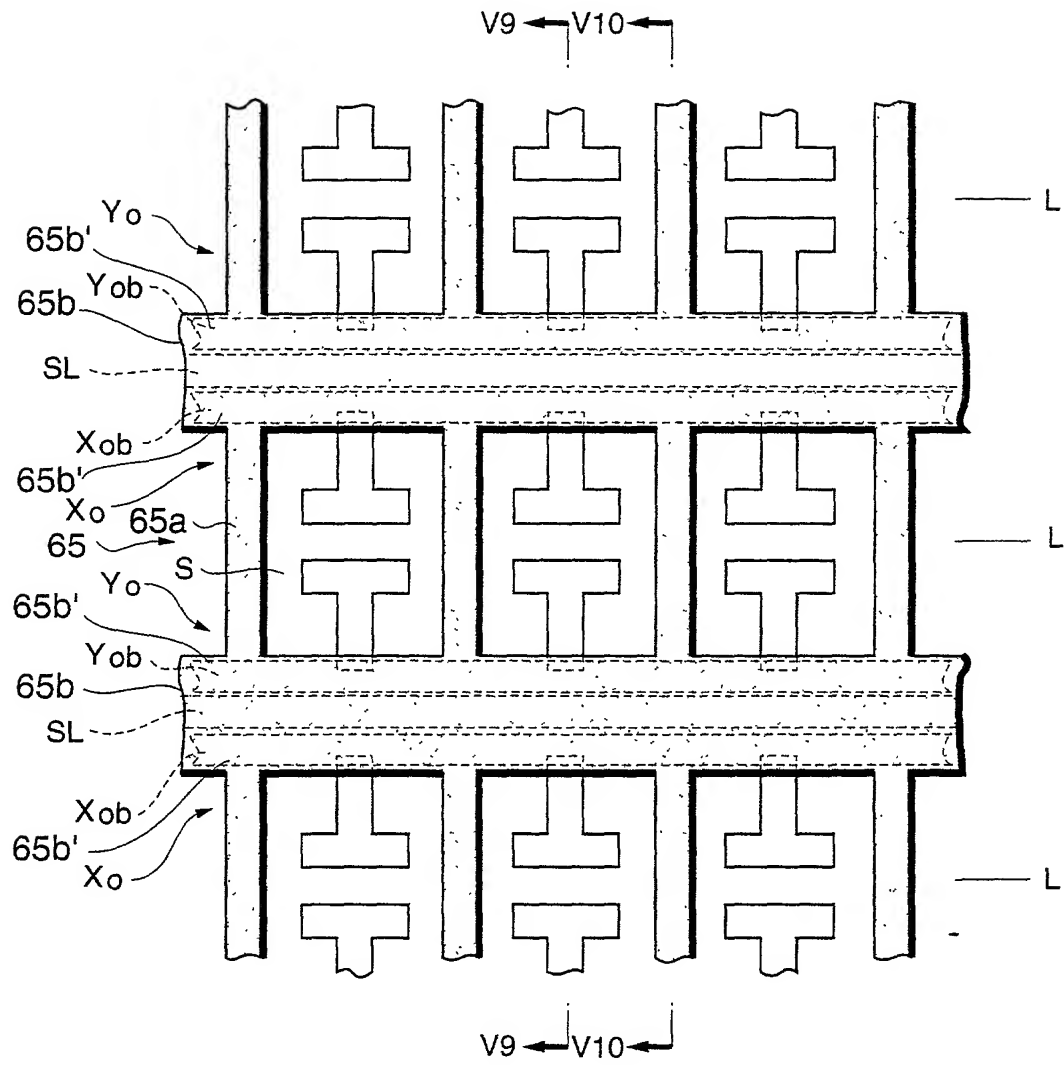
**Fig.21**

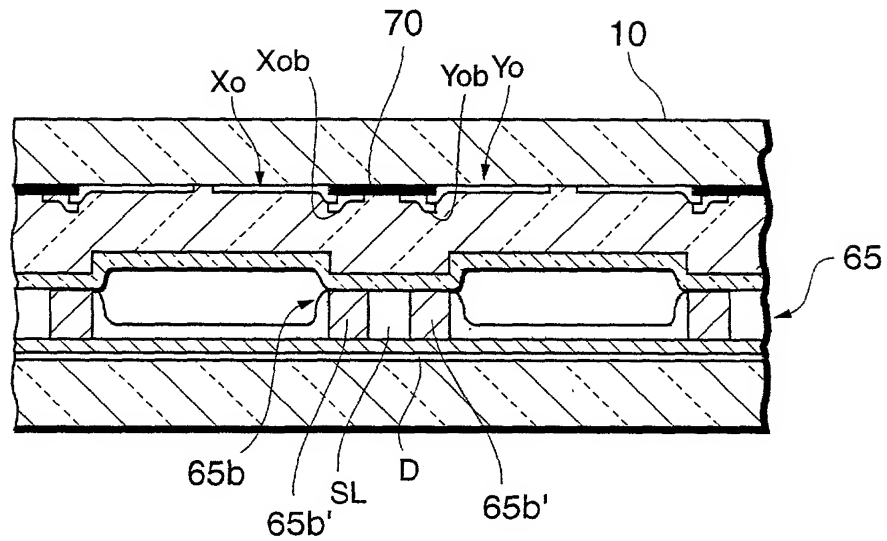
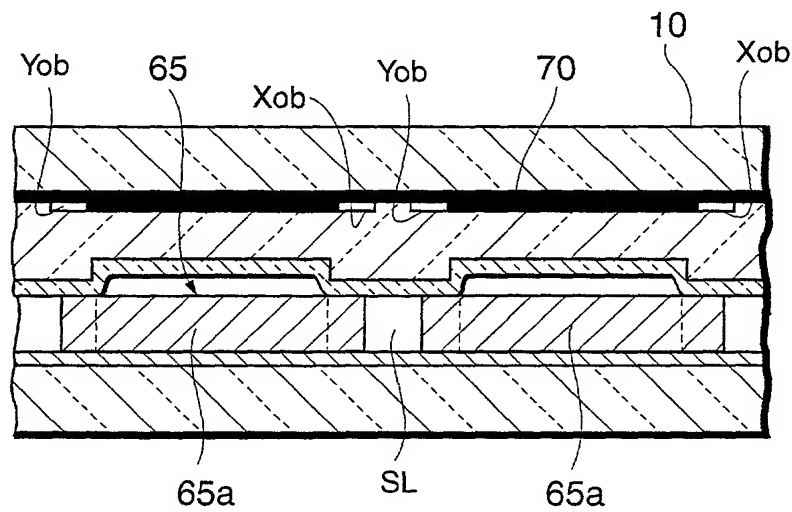


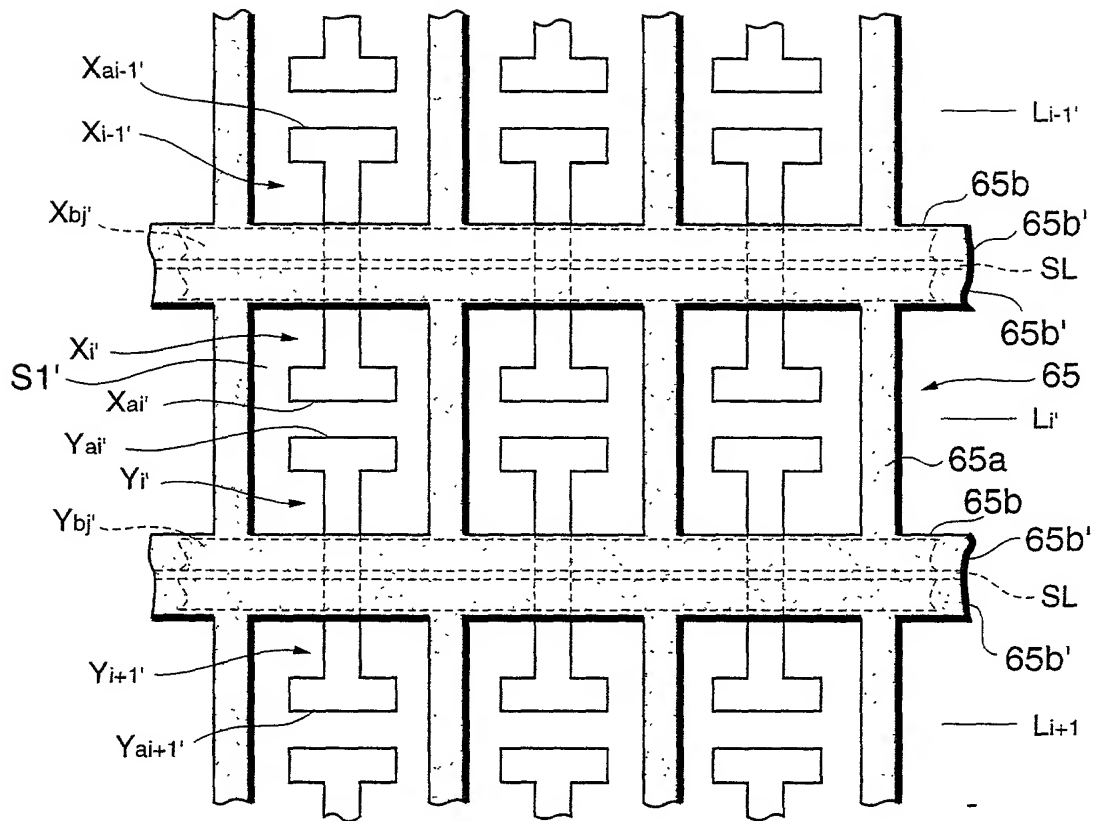
**Fig.22**

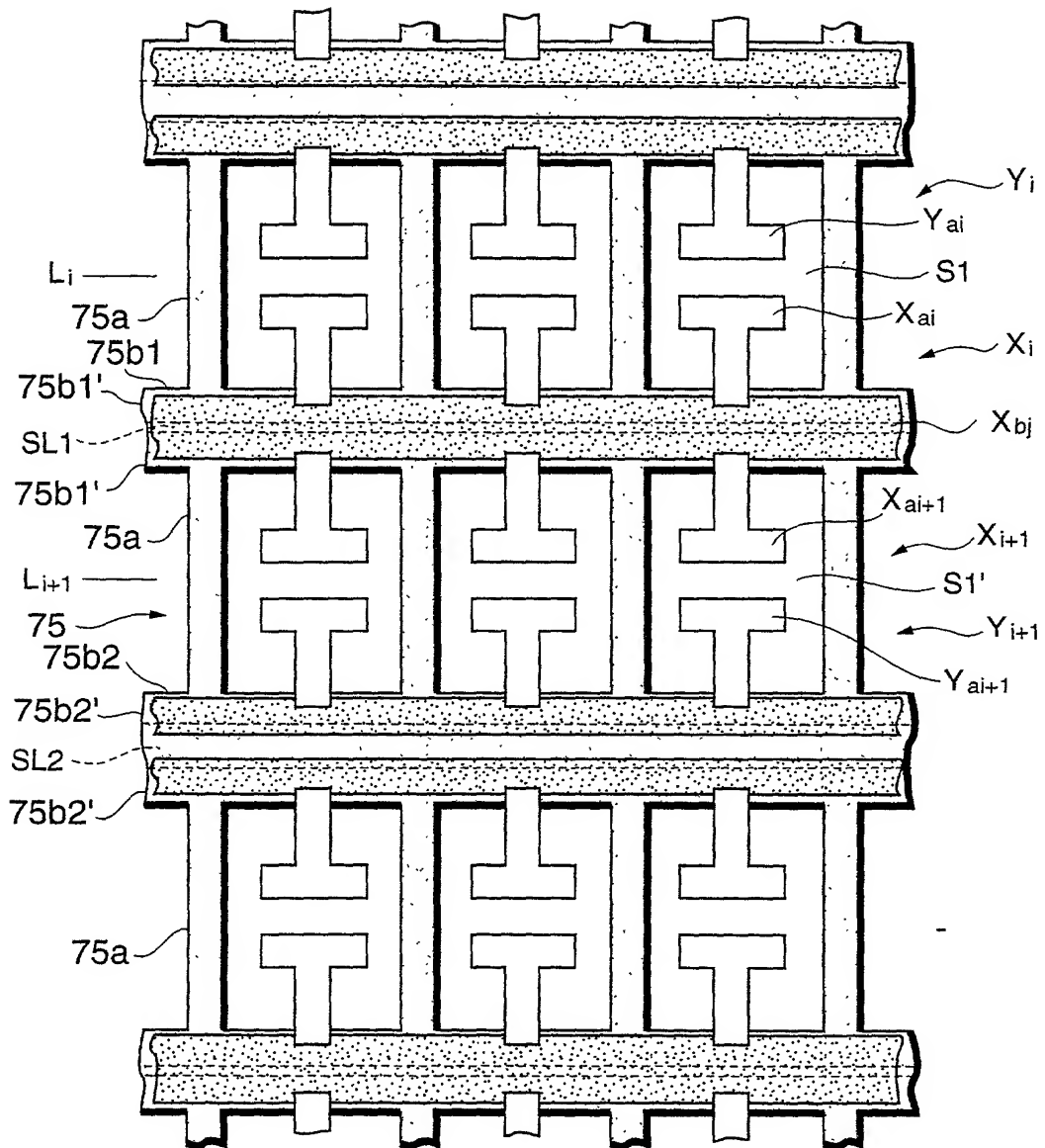
**Fig.23**V7-V7 SECTION**Fig.24**V8-V8 SECTION

**Fig.25**W5-W5 SECTION**Fig.26**W6-W6 SECTION

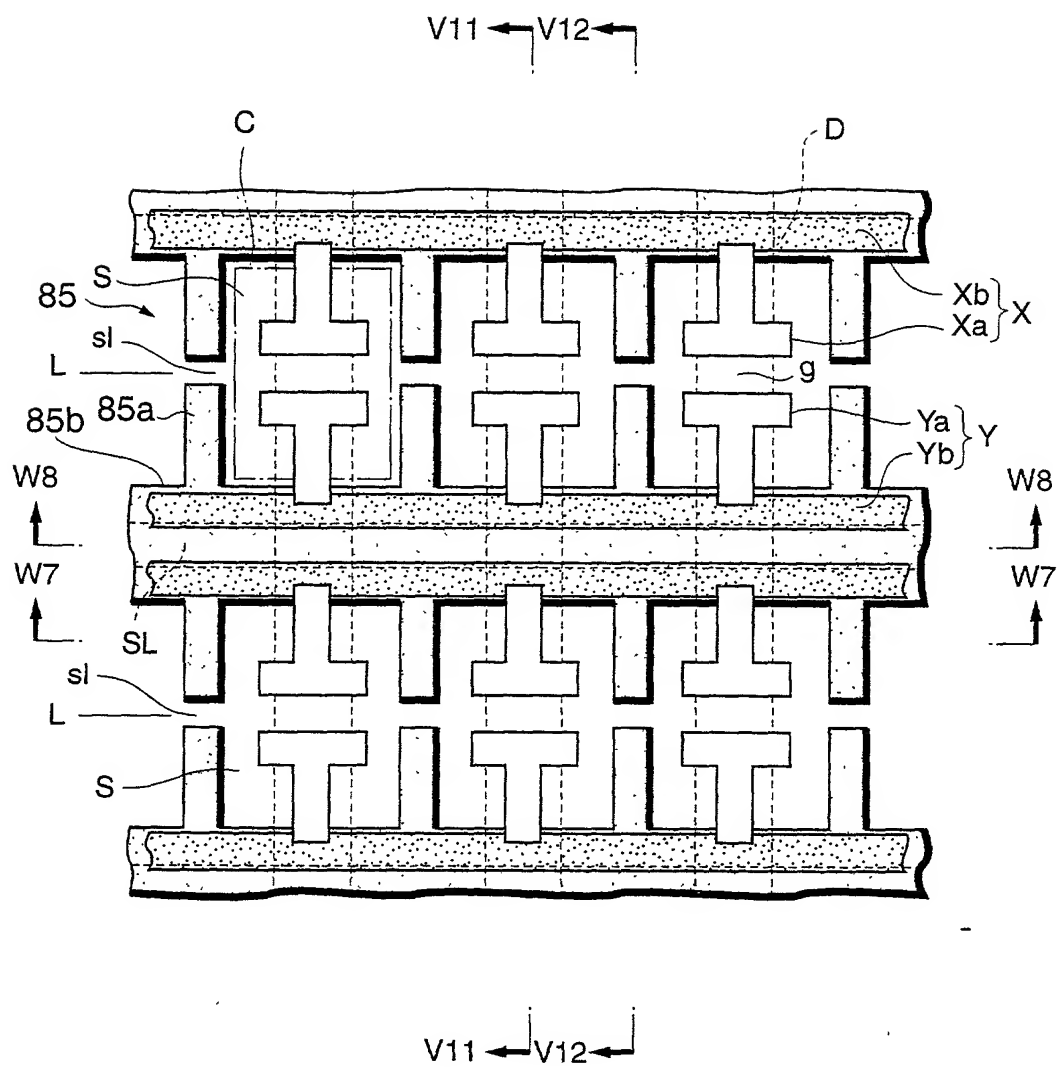
**Fig.27**

**Fig.28**V9-V9 SECTION**Fig.29**V10-V10 SECTION

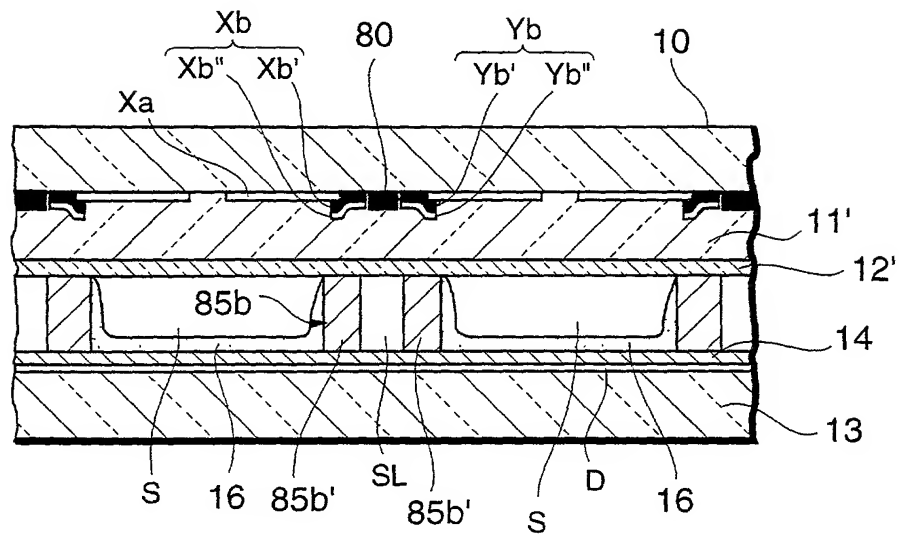
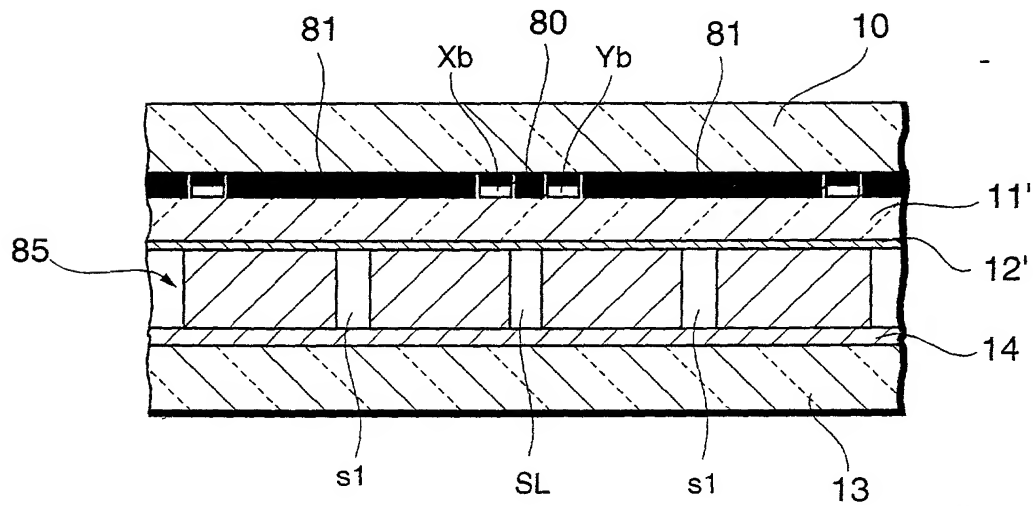
**Fig.30**

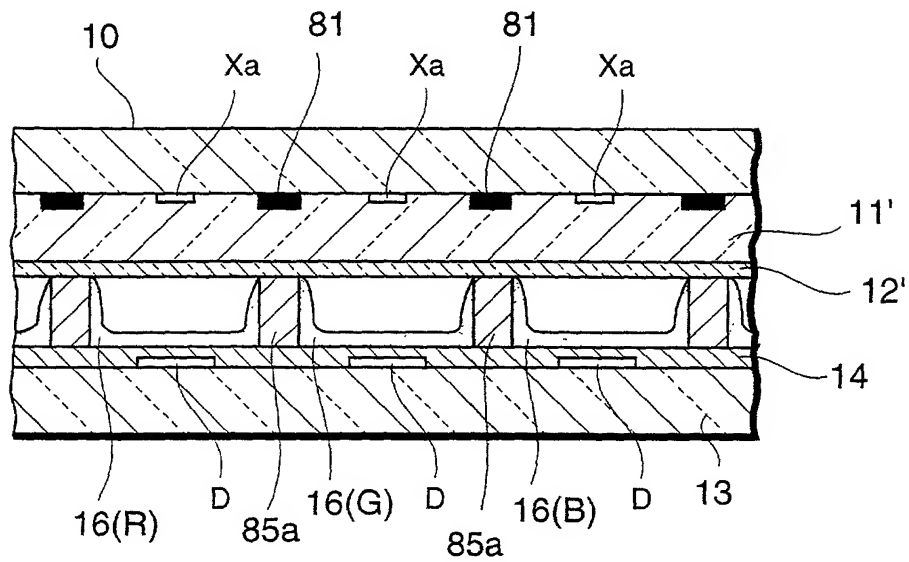
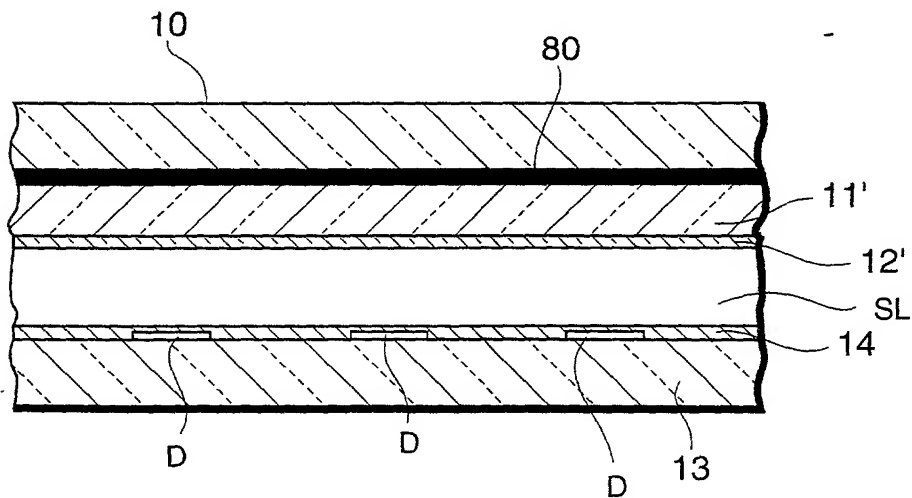
**Fig.31**

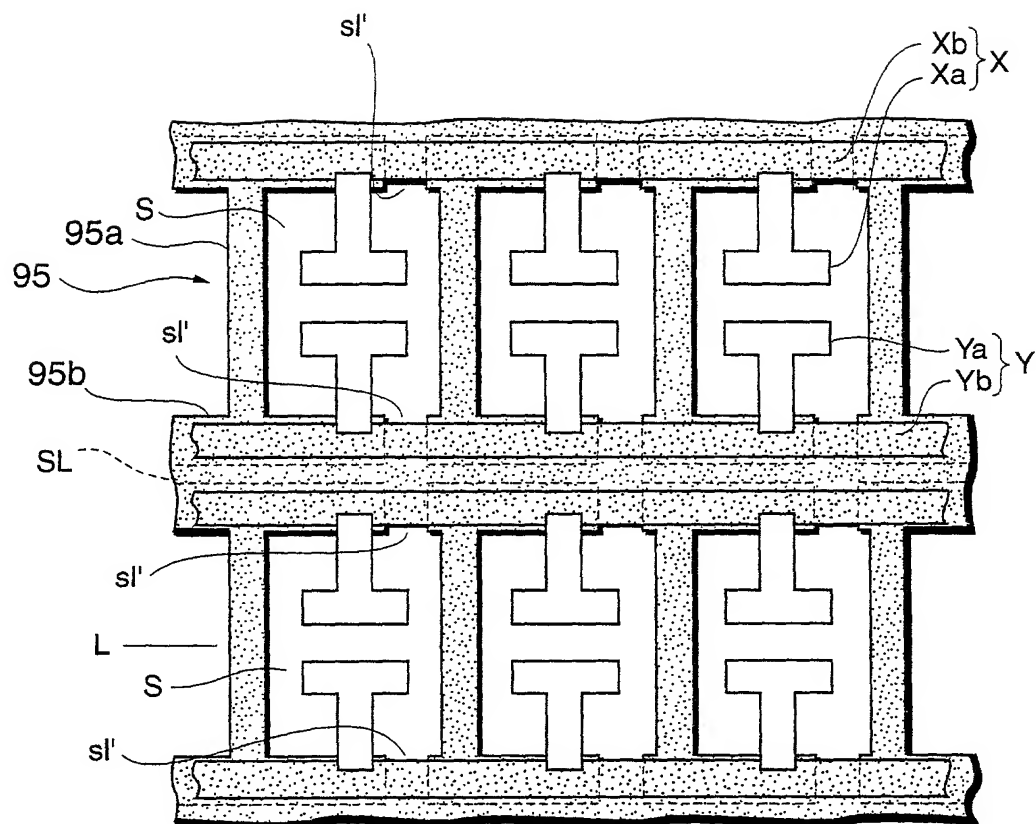
**Fig.32**

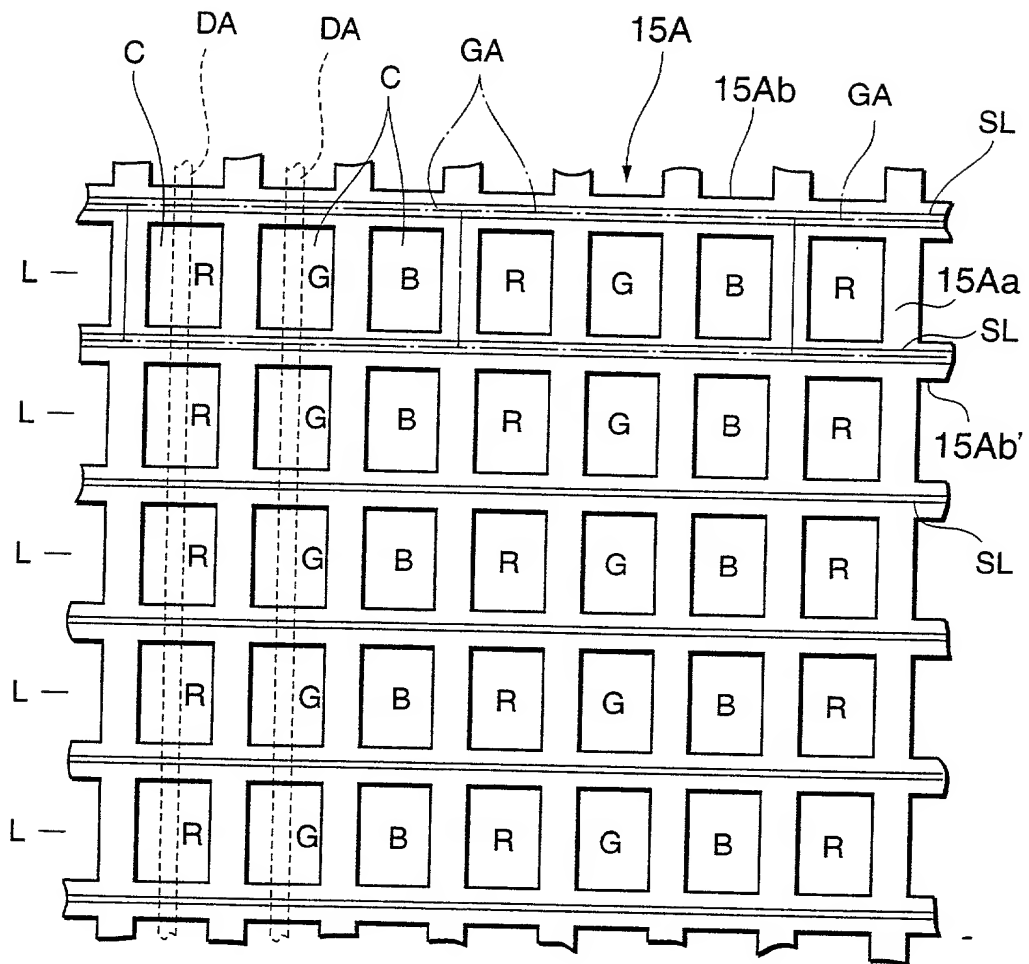


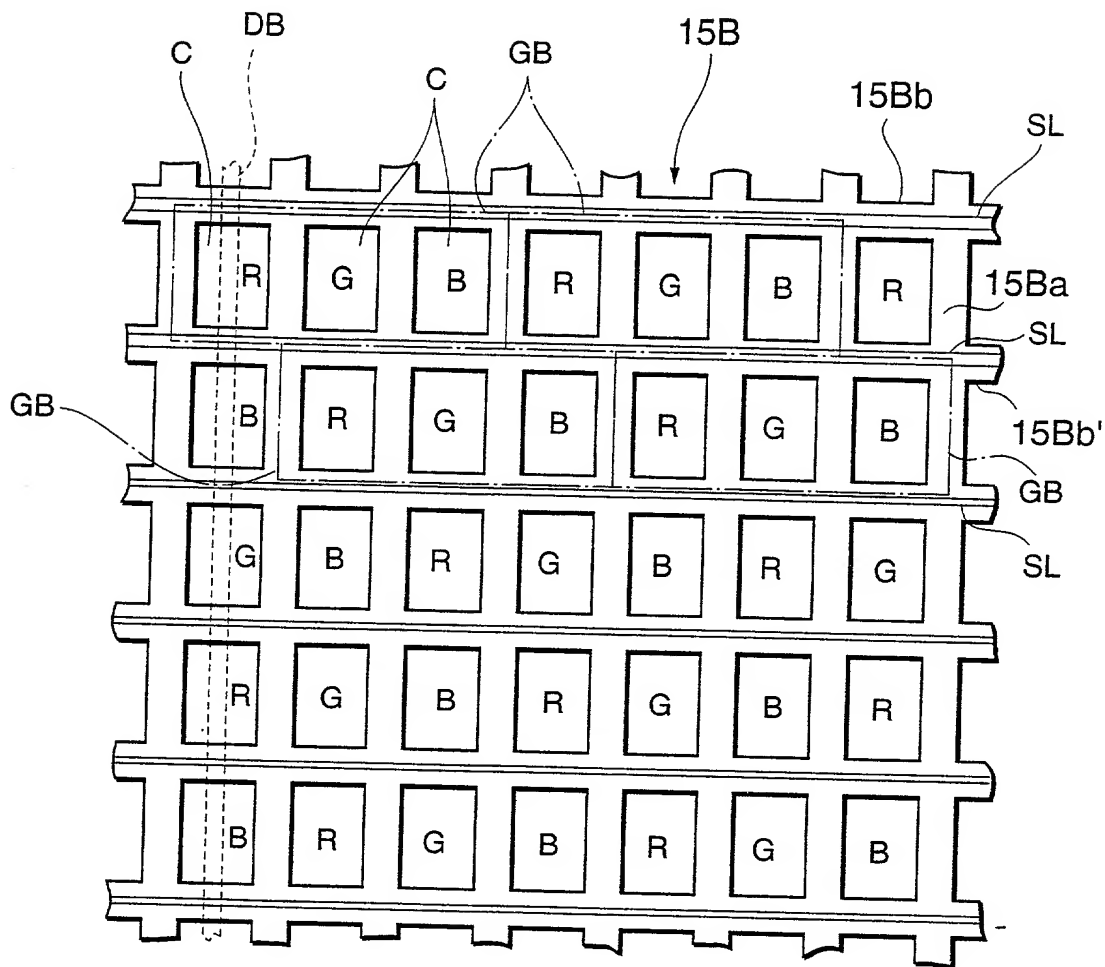


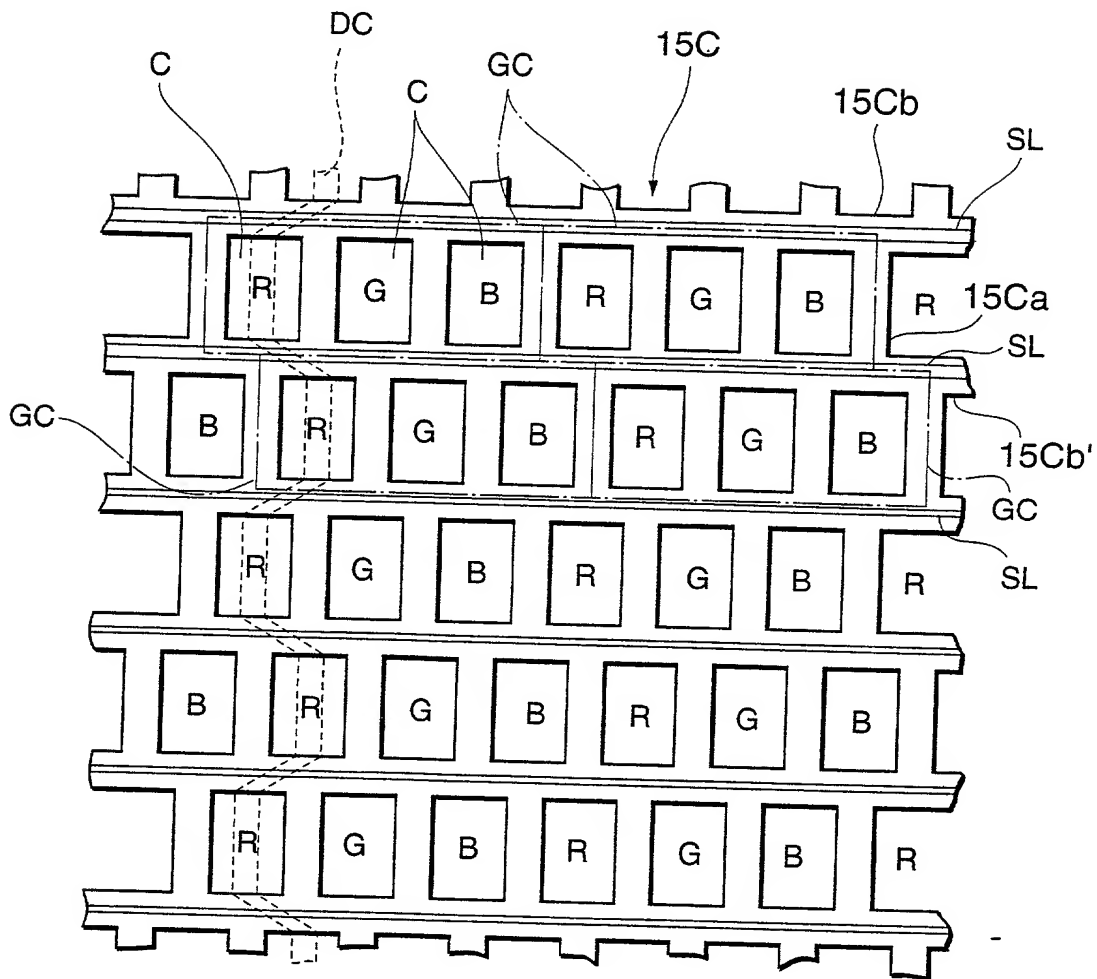
**Fig.33**V11-V11 SECTION**Fig.34**V12-V12 SECTION

**Fig.35**W7-W7 SECTION**Fig.36**W8-W8 SECTION

**Fig.37**

**Fig.38**

**Fig.39**

**Fig.40**

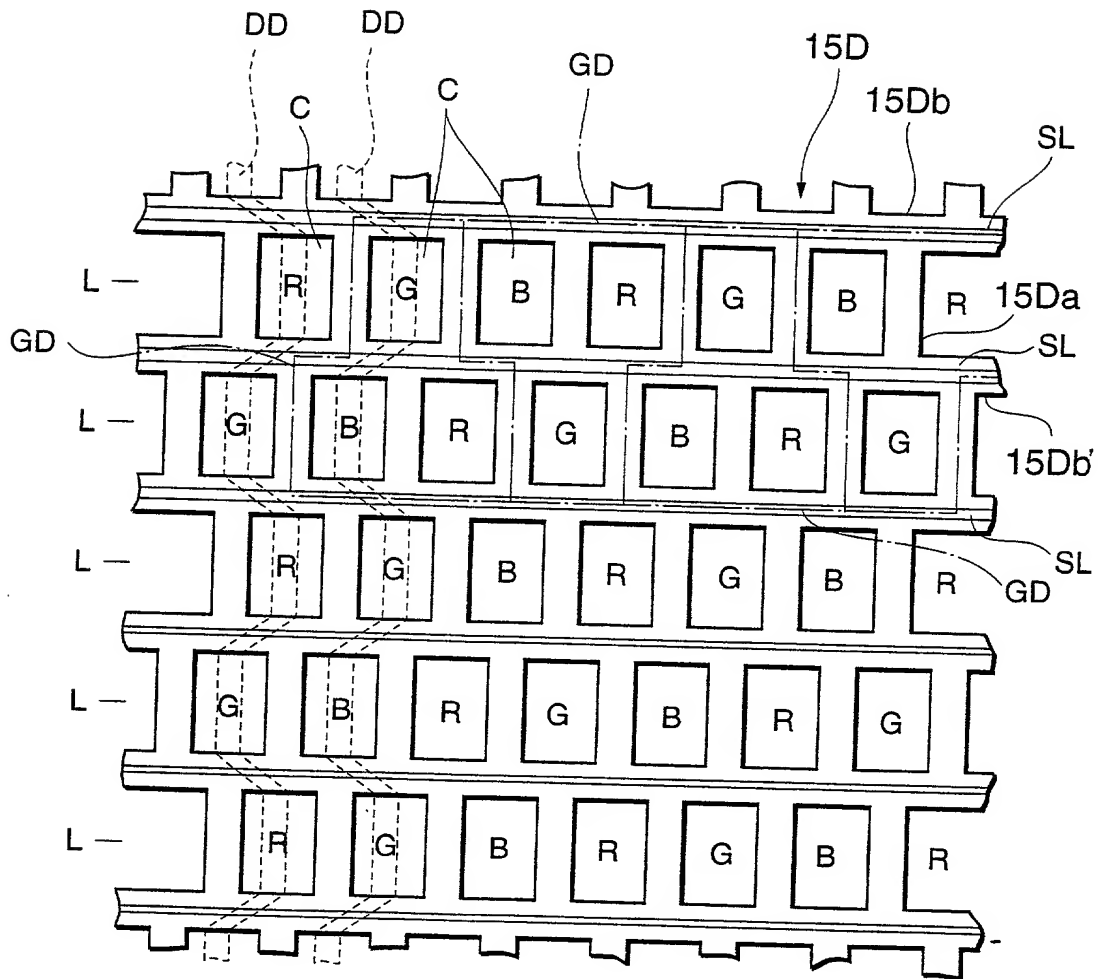
**Fig.41**

Fig. 42

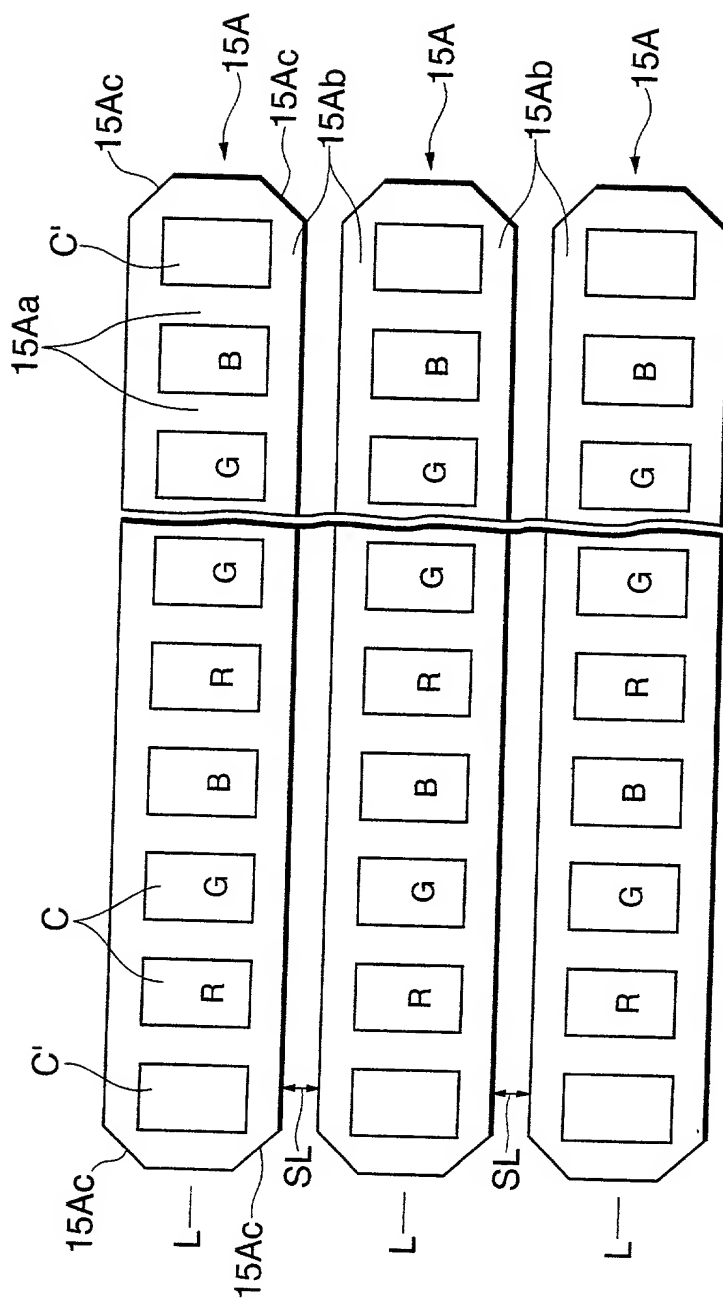
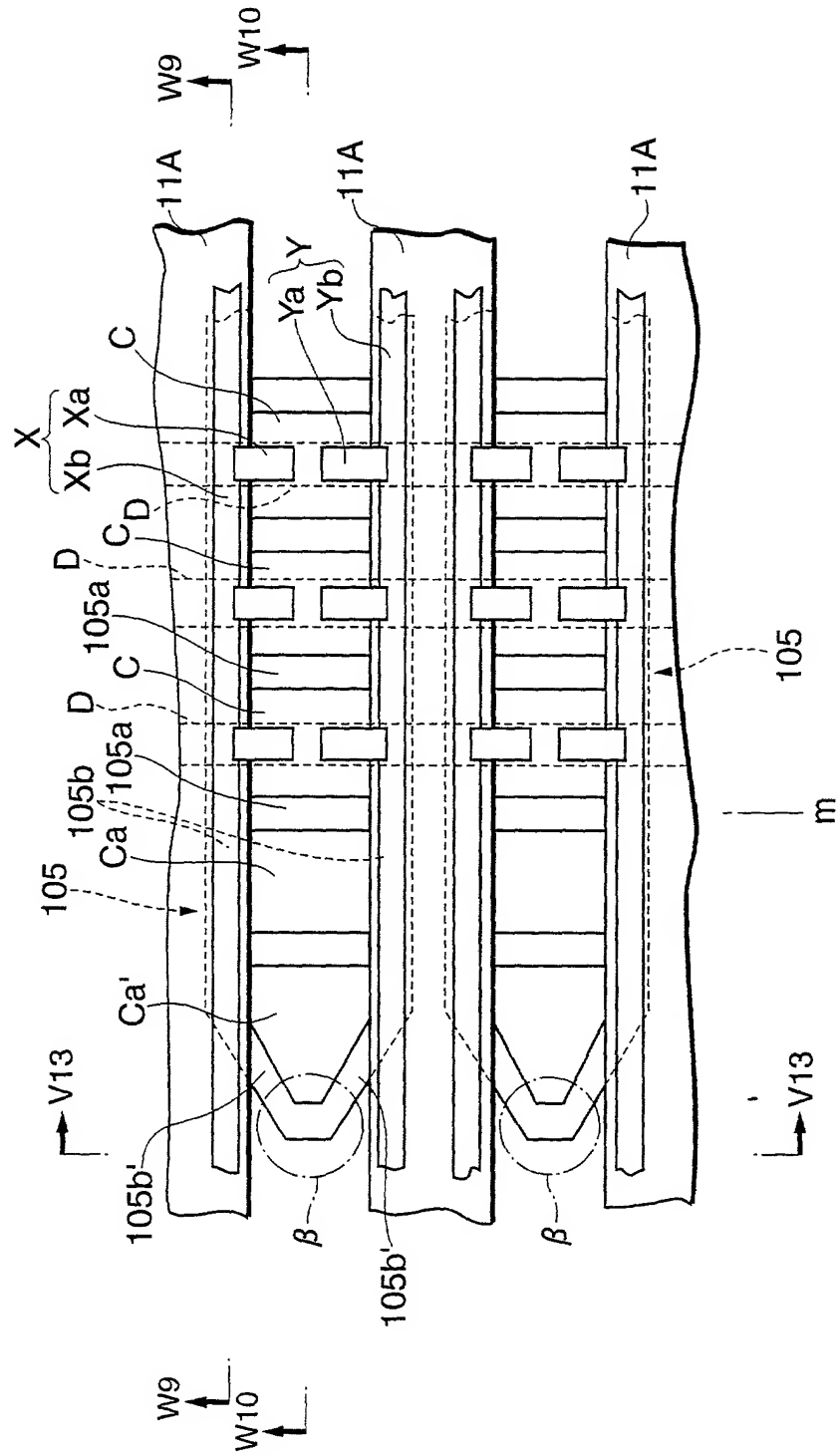
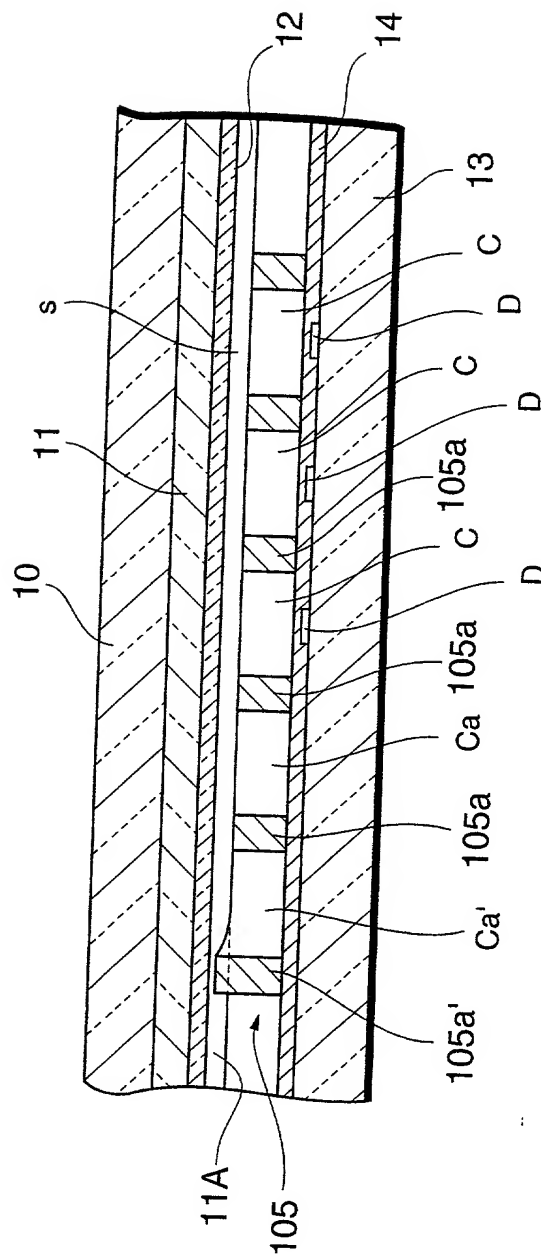


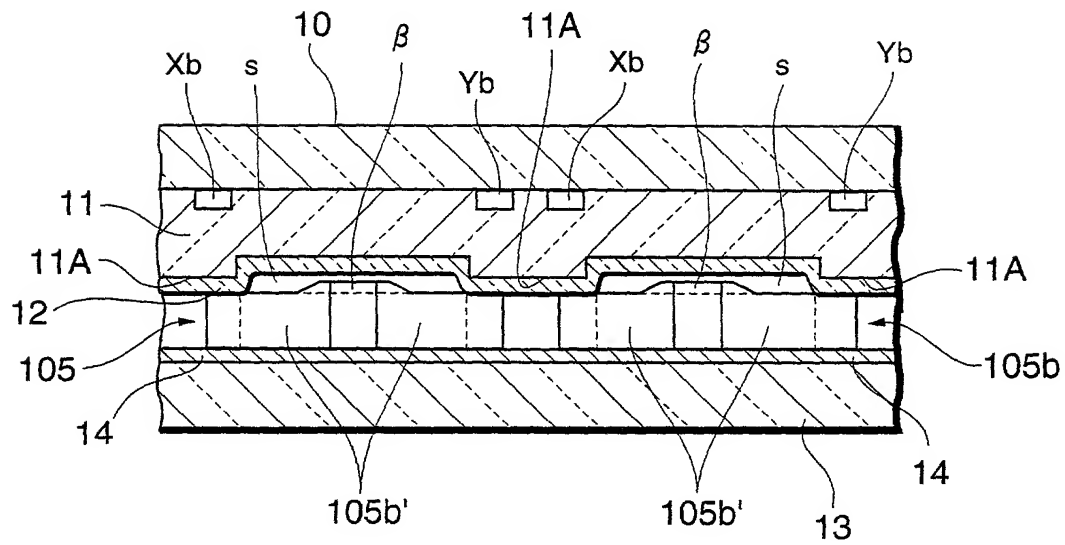


Fig. 43



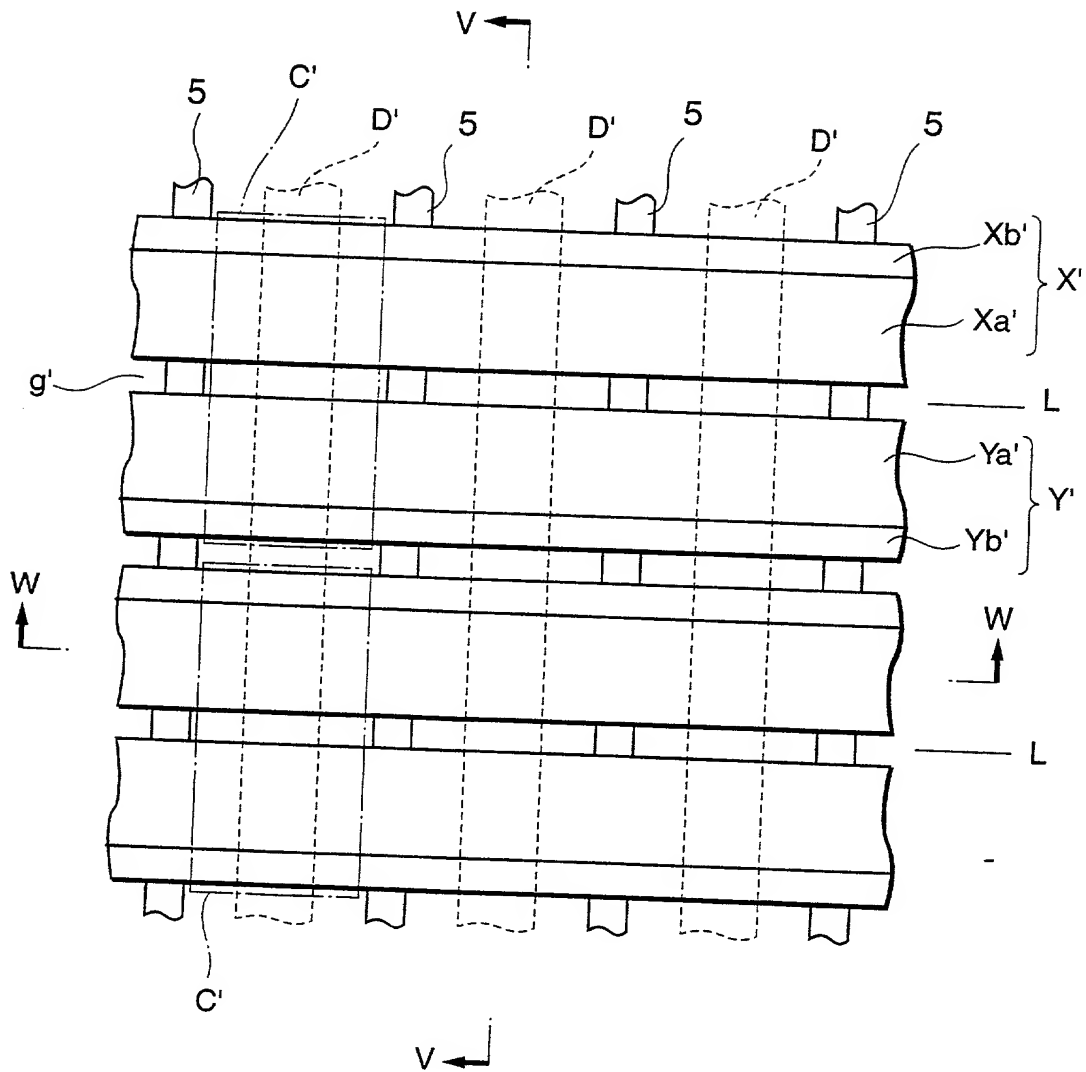


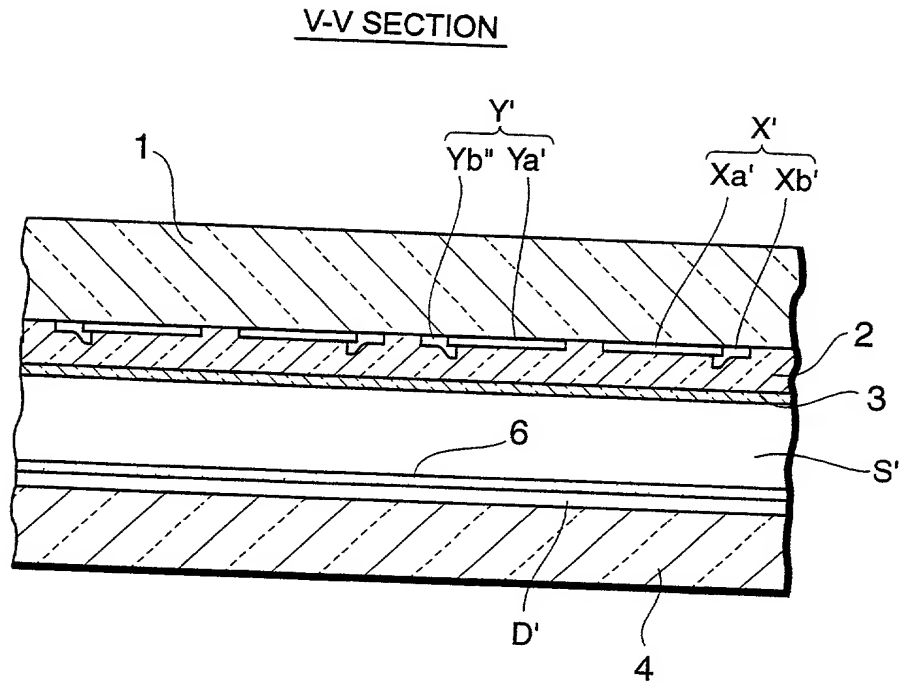
W10-W10 SECTION

**Fig.46**V 1 3 - V 1 3 SECTION

**Fig.47**

(PRIOR ART)



**Fig.48** (PRIOR ART)**Fig.49** (PRIOR ART)